MOSFET

Metal oxide semiconductor field effect transistor

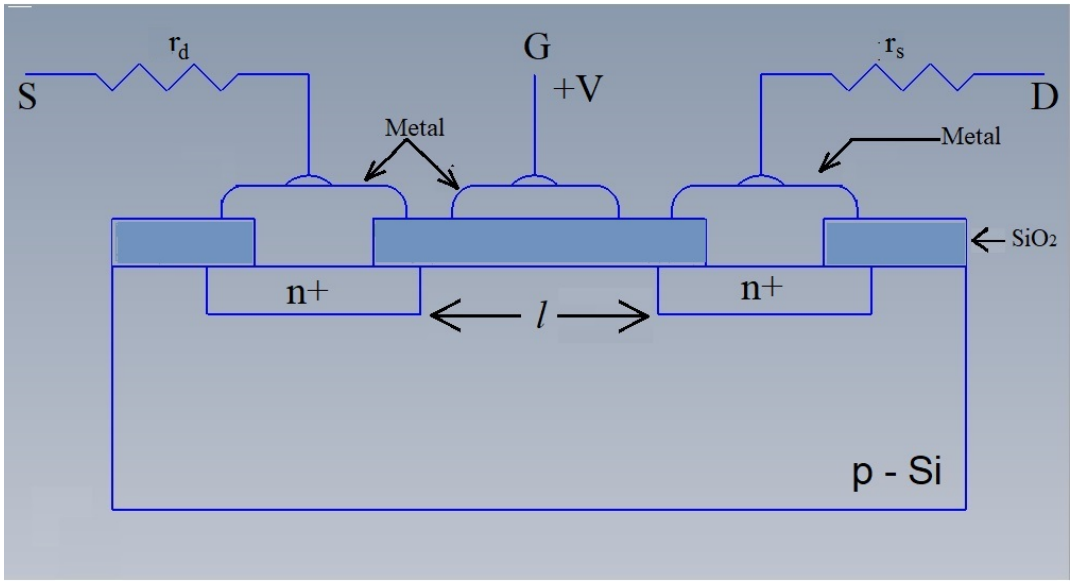


Fig.1 MOSFET Configuration

The configuration of this device is shown in Fig.1. the metallic electrode is completely insulated from the semiconductor electrode by means of a thin insulating layer in between. Owing to this ,the device is sometimes referred to as the insulated gate field effect transistor(IGFET).A positive voltage applied to the metallic gate electrode may induce a conducting channel in the semiconductor substrate under suitable circumstances.

In the planner configuration as shown in the figure 1 ,the two diffused n^+ regions on each side of the device serve as source (S) and the drain (D) electrodes.

To analyze the device operation ,we presume the complete absence of surface states from the semiconductor – insulator interface.

It is easy to note that without any gate voltage applied, no conduction through the channel is ever possible because of the placement of two pn junction back to back in series.

On applying positive bias on gate electrode ,holes underneath it in the p-channel tend to driven away towards bulk of the semiconductor, exposing the negative acceptor ions lying there.

When the gate bias is sufficiently increased ,all the available mobile holes are driven away from the from the interface. Then they expose all the negative ionic acceptor charges. When these charges are no longer able to compensate the effects of increasing positive gate bias, electrons are drawn towards the interface from the bulk semiconductor.

An interfacial layer of mobile electrons is then created, connecting source to drain. On applying a suitable drain-source voltage ,electric conduction through the channel then becomes possible. Now it is easy to note that any increase in the gate voltage (V_g) would give rise to an increase in the channel conductance.

Next to derive I-V relation we presume that the voltage at any point x the channel (measured along its length from drain end)is V(x),so that the transverse voltage across the insulator at the point would be [V_g-V(x)]

We however normally find V_g to be much higher compared to V(x),If the uniform thickness of the oxide layer is t , then the electric field intensity at that particular point becomes

$$\varepsilon(x) = [V_g - V(x)]/t$$

The surface charge density induced at the semiconductor insulator interface by this electric field as obtained from Gauss law of electrostatics is given by

$$\rho(x) = \varepsilon_i \varepsilon_0 \varepsilon(x)$$

Where ε_i measures the relative permittivity of the insulator. Mobile electrons along with immobile acceptor ions constitute ρ_i (x).

As such ,all the charges developed at the semiconductor insulator interface are not available for conduction. If we now define a part of applied voltage on the gate v_g as a characteristic voltage v_T (turn on voltage)when the channel conduction due to electrons just begins ,we may write

$$q\Delta n(x) = \varepsilon_i \varepsilon_0 [V_g - V(x) - V_T]/t$$

Where $\Delta n(x)$ measures the electron density developed per unit area of the insulator for the purposes of conduction. The thickness t of the insulator is related to the gate capacitance C_g in the following manner

$$C_g = \varepsilon_i \varepsilon_0 (lW)/t$$

Where W measures the width of the gate electrode normal to the plane of the paper. On substituting for.we get

$$q\Delta n(x) = (C_g / lW)[V_g - V(x) - V_T]$$

Next let us concentrate on a length Δx of the channel of unit thickness inside p-Si. Its conductance may then be expressed as

$$G(x) = \sigma(x)\frac{W.l}{\Delta x} = q\mu_n \Delta n(x)\frac{W}{\Delta x}$$

On substuting for qΔn(x),we get

$$G(x) = \frac{\mu_n C_g}{l}[V_g - V(x) - V_T]\frac{1}{\Delta x}$$

The channel current I_d under the influence of the drain voltage ΔV is given by

$$I_d = G(x)\Delta V = \frac{\mu_n C_g}{l}[V_g - V(x) - V_T]\frac{\Delta V}{\Delta x}$$

Integrating over the length l of channel, we get

$$I_d = \frac{\mu_n C_g}{l}[V_g - V_T - \frac{V_d}{2}]V_d$$

Where V_d measures the applied drain voltage. The parasitic resistances associated with source and drain contacts may if the doping levels of n^+ regions forming the source and the drain are relatively higher.

Imposing $dI_d/dV_d=0$ in equn.,we may find that the drain current saturate s when $V_d=(V_g-V_T)$. The saturated drain current I_{ds} from is then given by

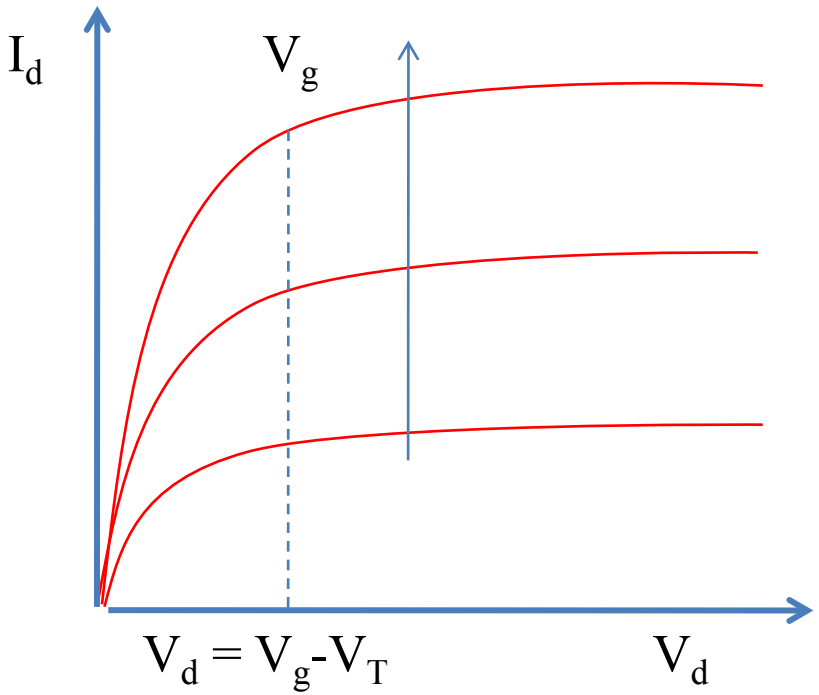
$$I_{ds} = \frac{\mu_n C_g}{l^2}\frac{(V_g - V_T)^2}{2}$$

Now the transconductance g_m in the saturated region may be obtained from

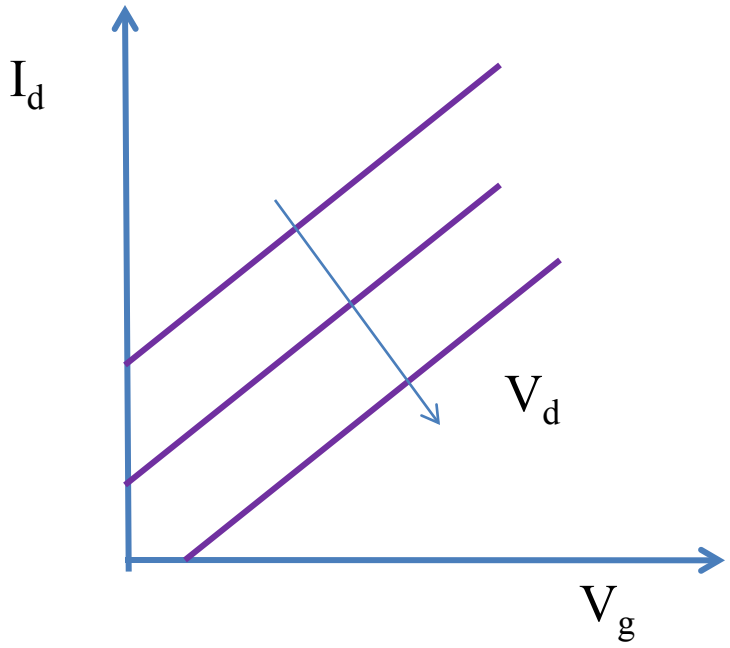
$$g_m = \left.\frac{\partial I_{ds}}{\partial V_g}\right|_{V_d} = \frac{\mu_n C_g}{l^2}(V_g - V_T)$$

The measured g_m is however found to be lower than that predicted by above equation. This is partly due to finite parasitic resistances r_s and r_d associated with the source and drain contacts and partly due to lowering of electron mobility owing to carrier scattering at oxide surfaces within the channel.

The plots of i_d- V_d and I_d- V_g curves are given in fig,2 drain current



Drain characteristics



Transfer characteristics

Because in this type of FET the drain current increases with drain voltage, it is said to operate in the enhancement mode. The conduction within the channel begins when the gate voltage applied to the insulator is just sufficient to generate an inversion layer within the channel. The gate turn-on voltage is called V_{GT}.

MESFET the metal semiconductor field effect transistor is identical in its operation to JFET and MOSFET. In it a Schottky barrier is used as gate electrode in place of a pn or a MIS junction ,It is some advantageous because of the low temperature required to formation of Schottky barrier and low channel resistance.