Timing Diagram

MCA 1ST YEAR 2ND SEMESTER 2020

Paper: MCA 203

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Timing Diagram is a graphical representation. It represents the execution time taken by each instruction in a graphical format. The execution time is represented in T-states.

Instruction Cycle:

The time required to execute an instruction .

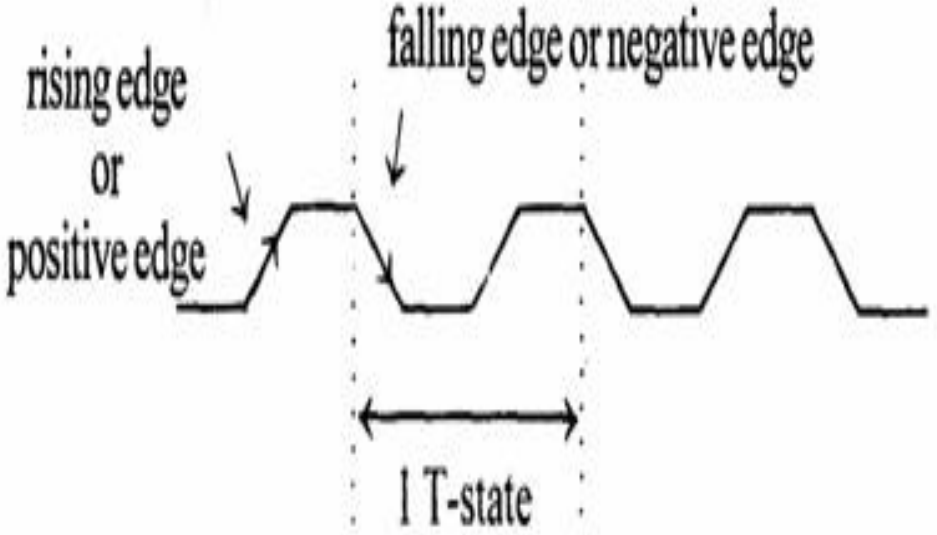
Machine Cycle:

The time required to access the memory or input/output devices .

T-State:

- The machine cycle and instruction cycle takes multiple clock periods.
- A portion of an operation carried out in one system clock period is called as T-state.

Note : *Time period, T = 1/f ; where f = Internal clock frequency*



Timing diagrams

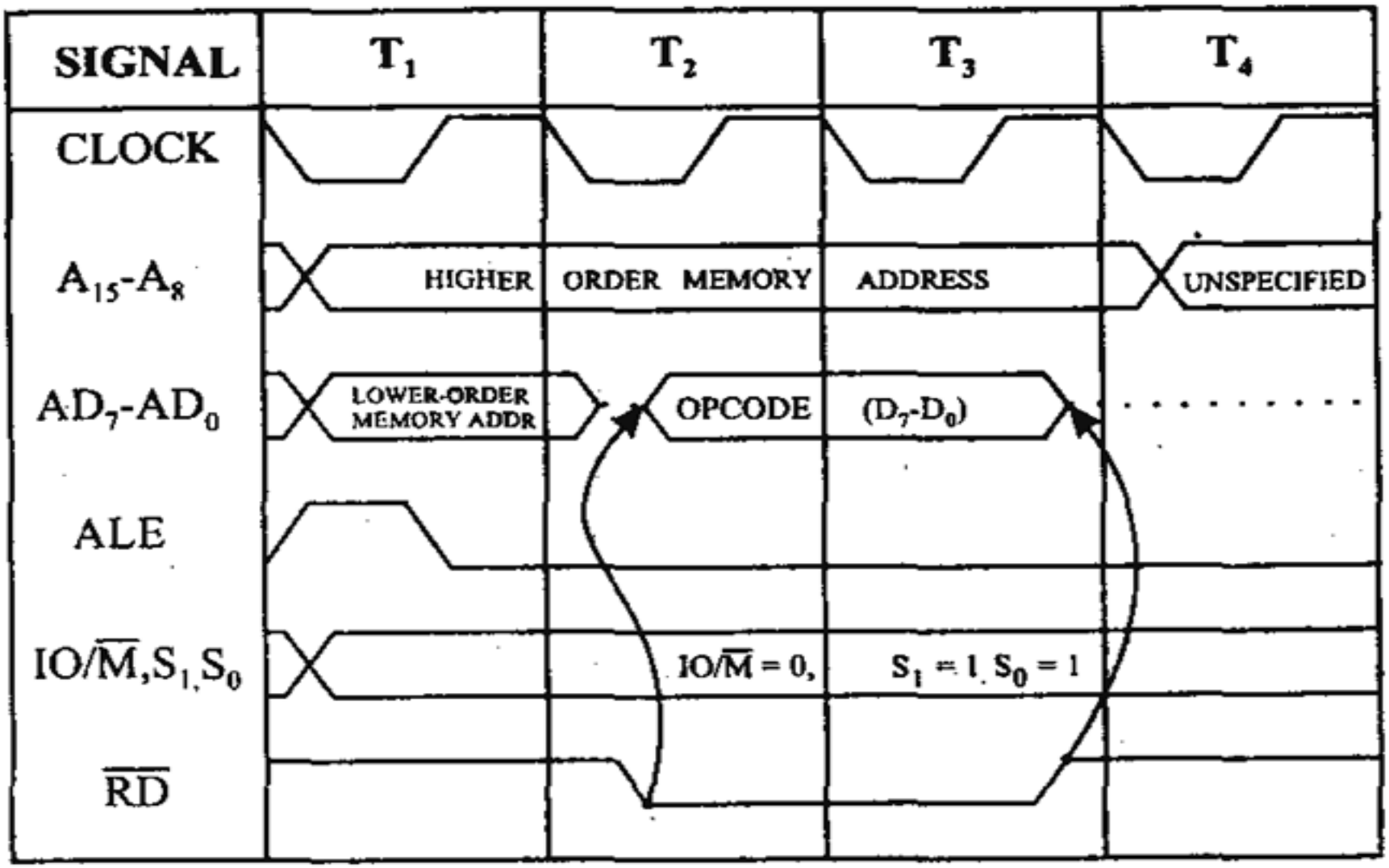
- The 8085 microprocessor has 7 basic machine cycle. They are

1. Op-code Fetch cycle(4T or 6T).
2. Memory read cycle (3T)
3. Memory write cycle(3T)
4. I/O read cycle(3T)
5. I/O write cycle(3T)
6. Interrupt Acknowledge cycle(6T or 12T)
7. Bus idle cycle

Machine Cycle	Status			No. of Machine cycles	Control
	IO/$\overline{M}$	S1	S0		
Opcode Fetch	0	1	1	4	$\overline{RD}$ =0
Memory Read	0	1	0	3	$\overline{RD}$ =0
Memory Write	0	0	1	3	$\overline{WR}$ =0
I/O Read	1	1	0	3	$\overline{RD}$ =0
I/O Write	1	0	1	3	$\overline{WR}$ =0
INTR Acknowledge	1	1	1	3	$\overline{INTA}$ =0

- Following Buses and Control Signals must be shown in a Timing Diagram:
- Higher Order Address Bus.
- Lower Address/Data bus
- ALE
- RD
- WR
- IO/M

Opcode fetch cycle(4T or 6T)



Opcode Fetch

- The Opcode fetch cycle, fetches the instructions from memory and delivers it to the instruction register of the microprocessor
- Opcode fetch machine cycle consists of **4 T-states**.

T1 State:

During the T1 state, the contents of the program counter are placed on the 16 bit address bus. The higher order 8 bits are transferred to address bus (A8-A15) and lower order 8 bits are transferred to multiplexed A/D (AD0-AD7) bus.

ALE (address latch enable) signal goes **high**. As soon as ALE goes high, the memory latches the AD0-AD7 bus. At the middle of the T state the **ALE goes low**

T2 State:

During the beginning of this state, the **RD' signal goes low** to enable memory. It is during this state, the selected memory location is placed on D0-D7 of the Address/Data multiplexed bus.

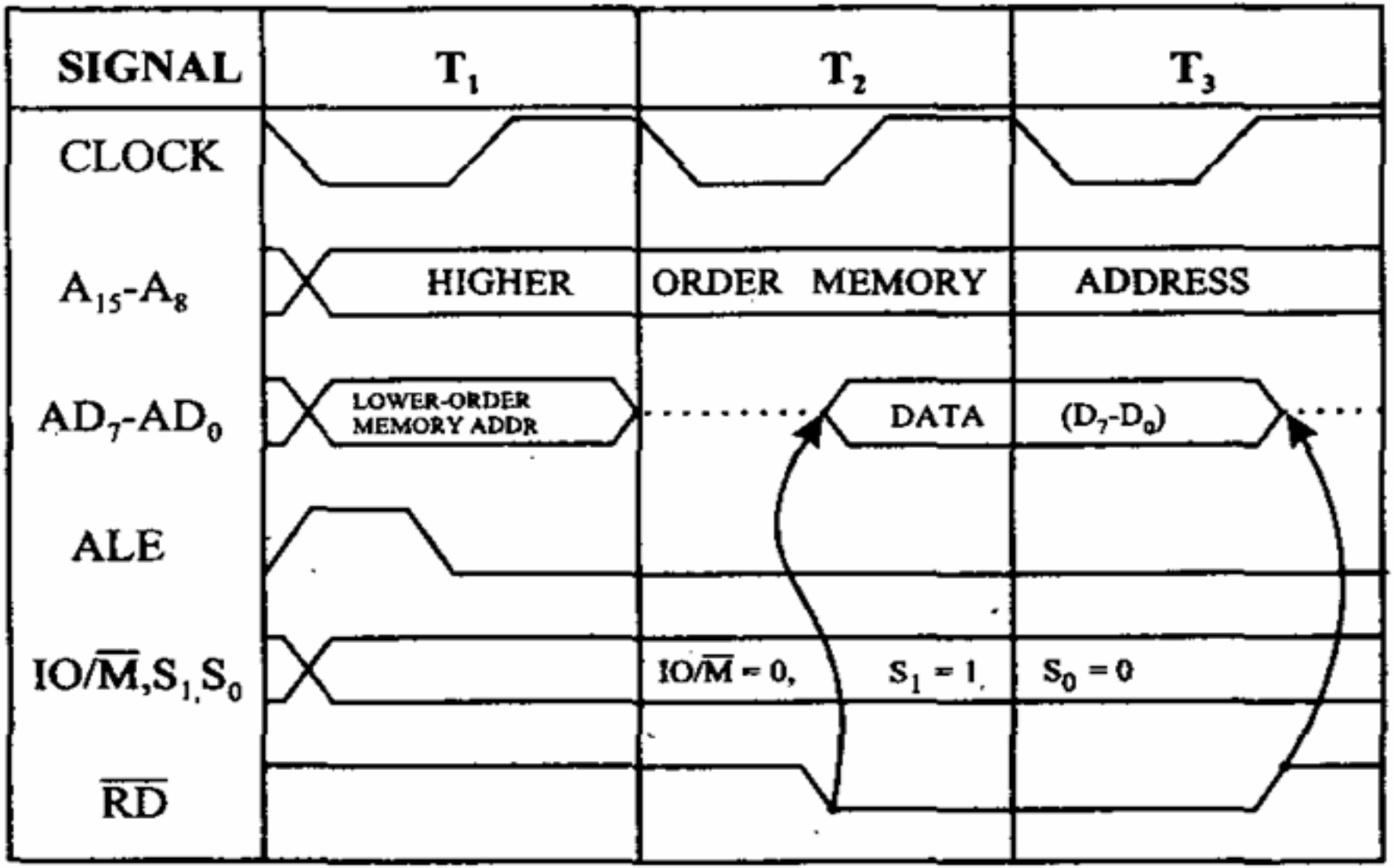
T3 State:

In the previous state the Opcode is placed in D0-D7 of the A/D bus. In this state of the cycle, the Opcode of the A/D bus is transferred to the instruction register of the microprocessor. Now the **RD' goes high** after this action and thus disables the memory from A/D bus.

T4 State:

In this state the Opcode which was fetched from the memory is decoded.

Memory read cycle (3T)



- These machine cycles have 3 T-states.

T1 state:

- The higher order address bus **(A8-A15)** and lower order address and data multiplexed (AD0-AD7) bus. **ALE goes high** so that the memory latches the (AD0-AD7) so that complete 16-bit address are available.

  The mp identifies the memory read machine cycle from the status signals **IO/M'=0, S1=1, S0=0**. This condition indicates the memory read cycle.

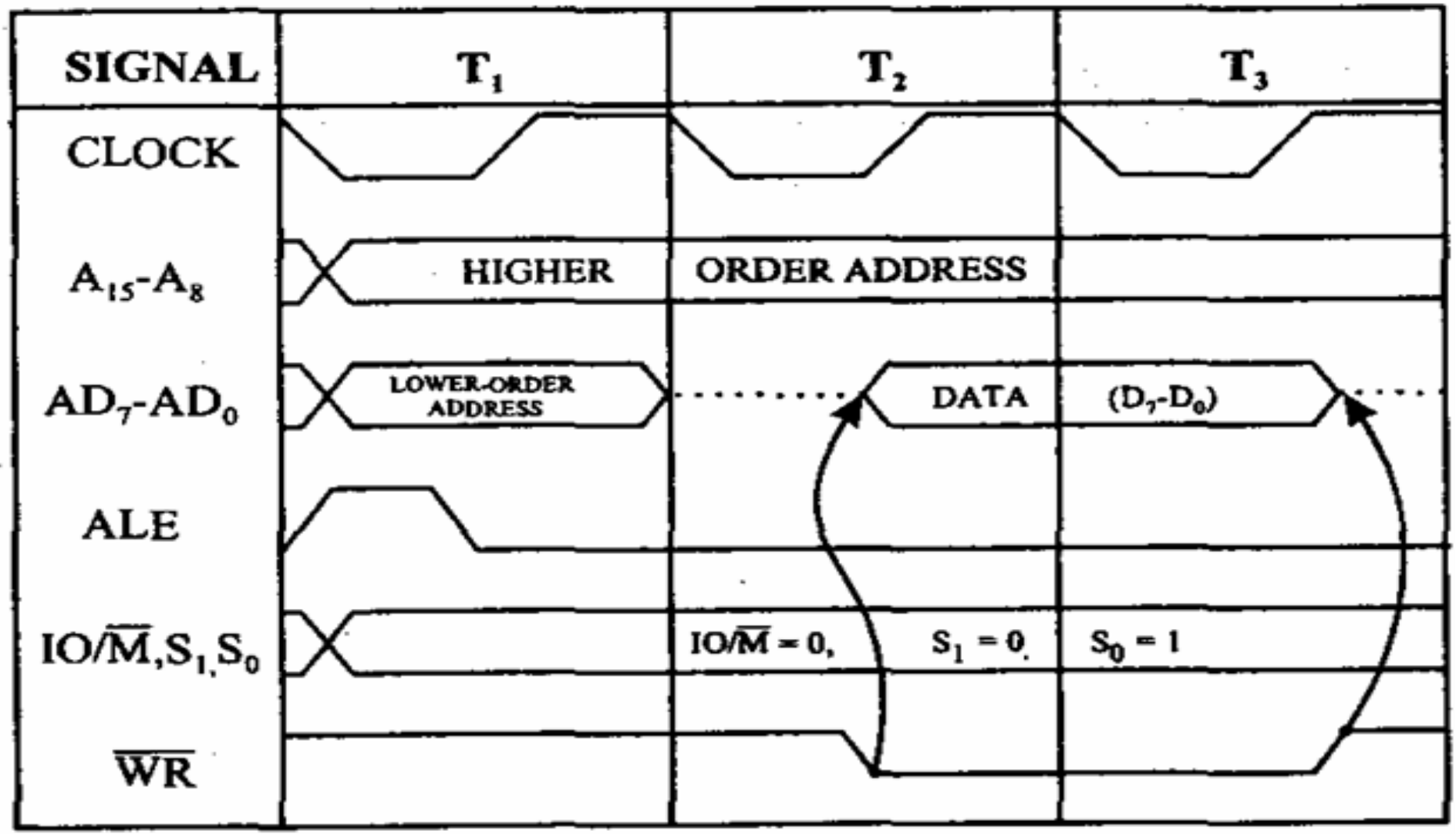
T2 state:

- Selected memory location is placed on the (D0-D7) of the A/D multiplexed bus. RD' goes **LOW**

T3 State:

- The data which was loaded on the previous state is transferred to the microprocessor. In the middle of the T3 state RD' goes high and disables the memory read operation. The data which was obtained from the memory is then decoded.

Memory write cycle (3T)



- These machine cycles have 3 T-states.

T1 state:

- The higher order address bus **(A8-A15)** and lower order address and data multiplexed (AD0-AD7) bus. **ALE goes high** so that the memory latches the (AD0-AD7) so that complete 16-bit address are available.

  The mp identifies the memory read machine cycle from the status signals **IO/M'=0, S1=0, S0=1**. This condition indicates the memory read cycle.

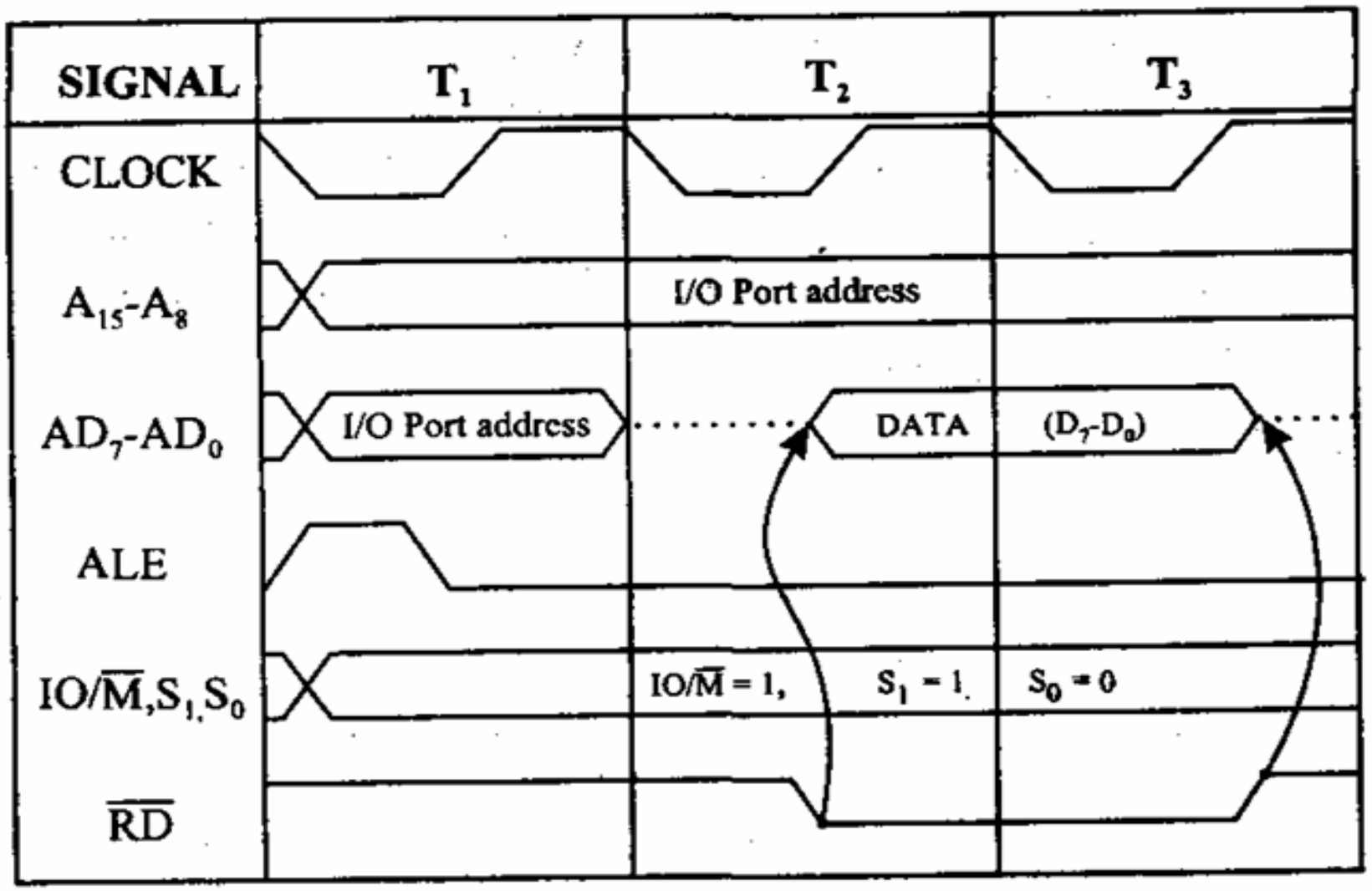
T2 state:

- Selected memory location is placed on the (D0-D7) of the A/D multiplexed bus. WR' goes **LOW**

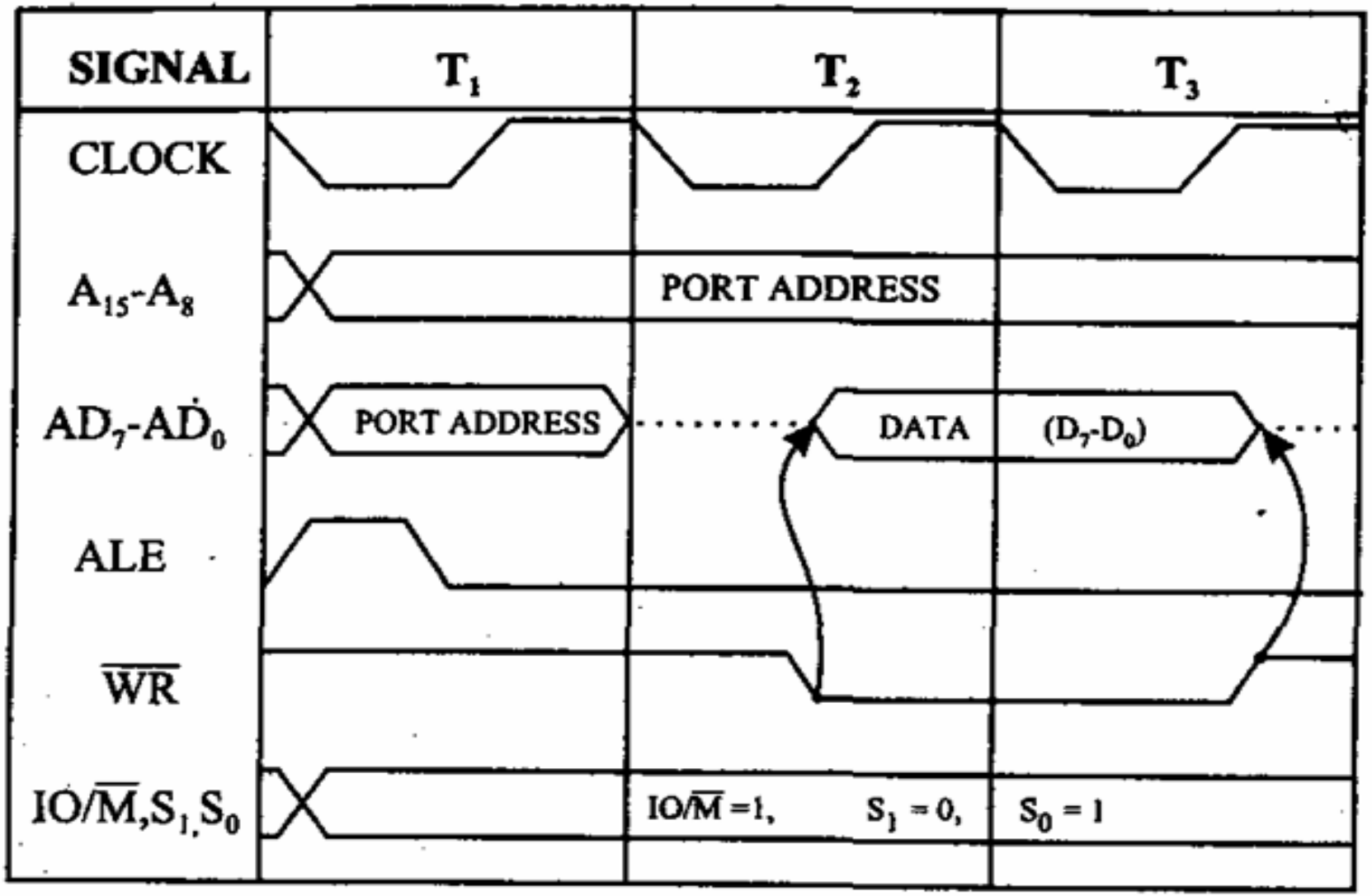
T3 State:

- In the middle of the T3 state WR' goes high and disables the memory write operation. The data which was obtained from the memory is then decoded.

I/O read cycle(3T)



I/O write cycle(3T)

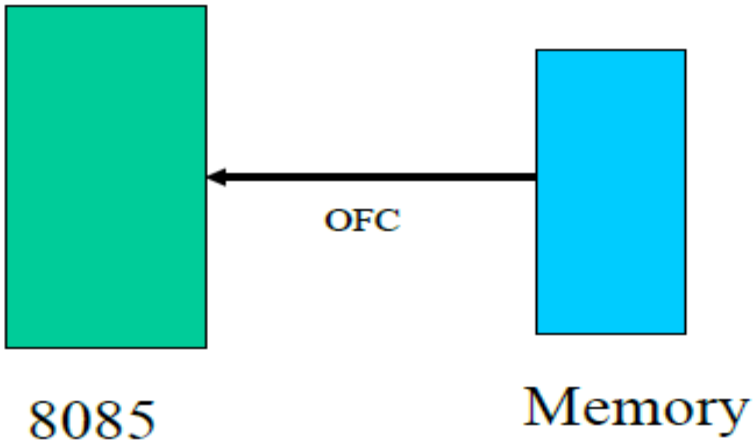


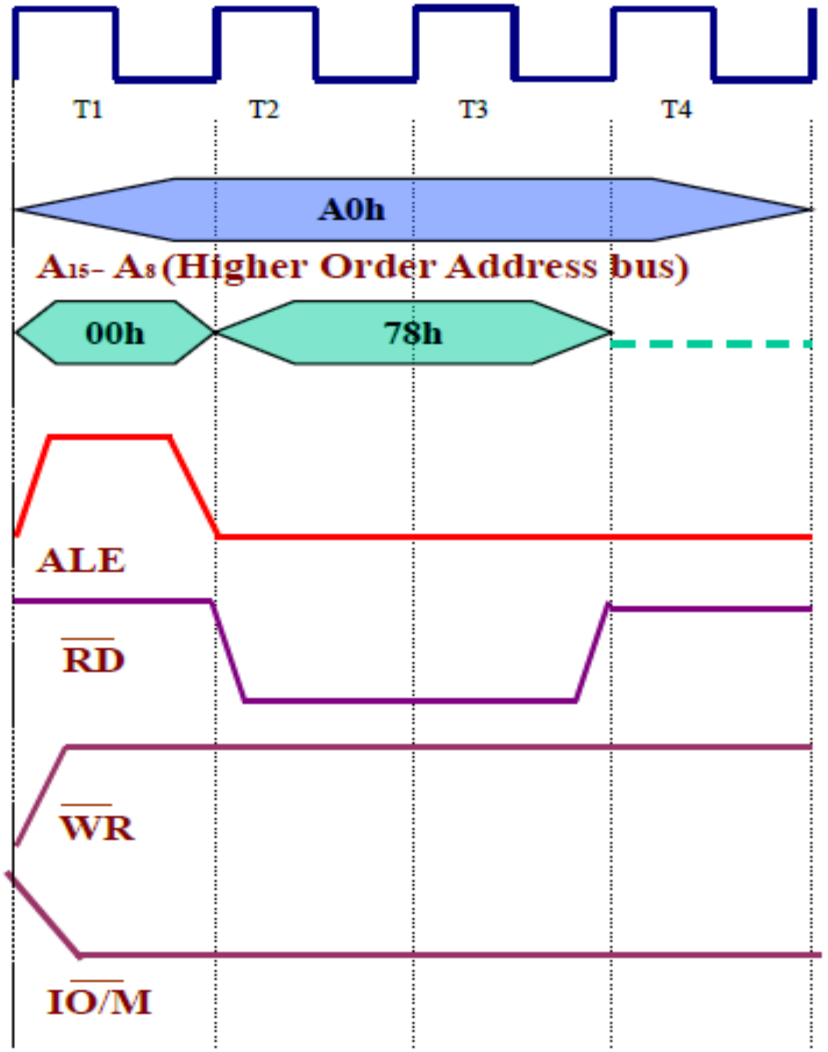
Instruction:

A000h MOV A,B

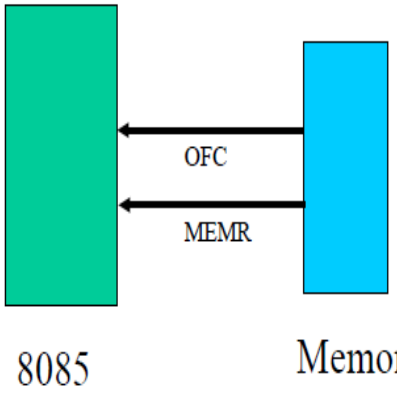
Corresponding Coding:

A000h 78





Op-code fetch Cycle



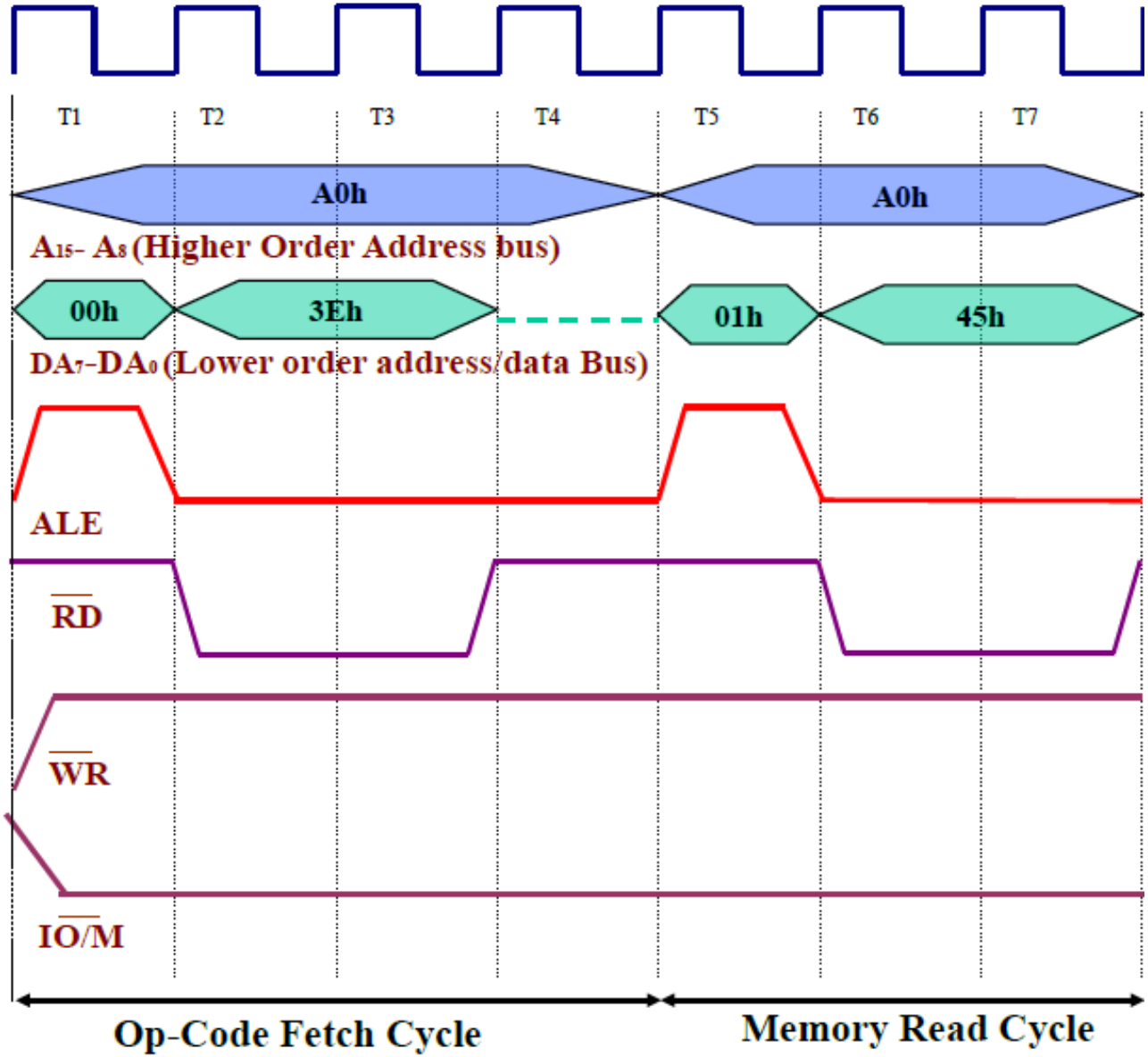
Instruction:

A000h MVI A,45h

Corresponding Coding:

A000h 3E

A001h 45



Instruction:

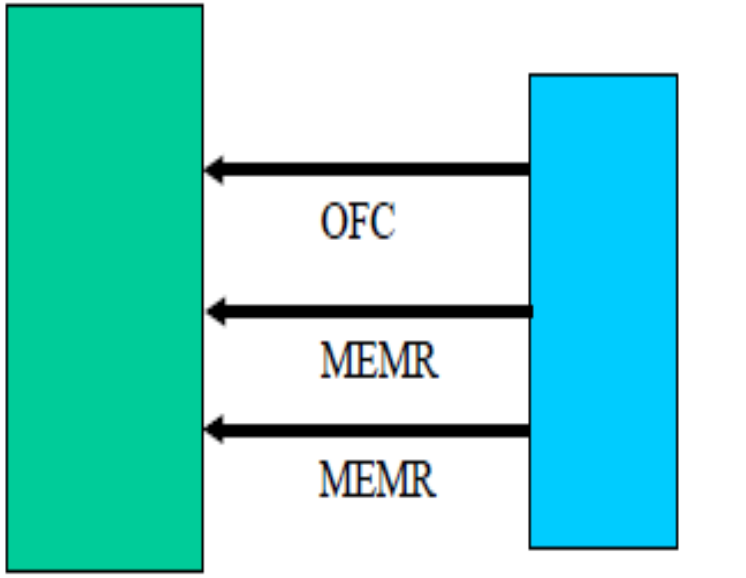
A000h LXI A,FO45h

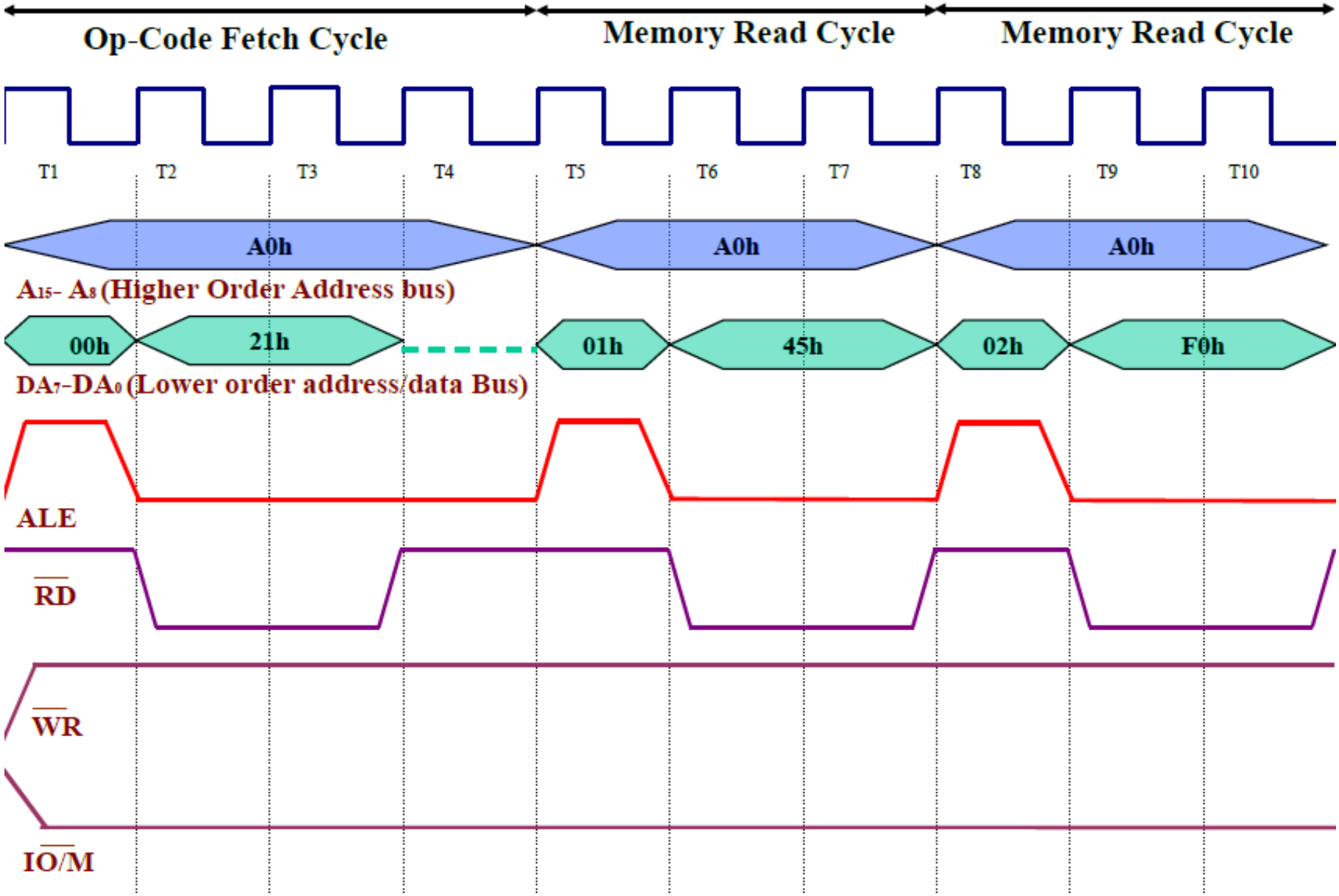
Corresponding Coding:

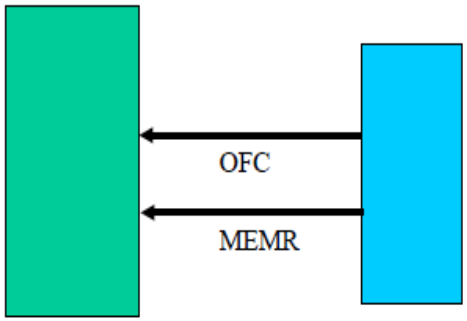
A000h 21

A001h 45

A002h F0




Op-Code Fetch Cycle
Memory Read Cycle
Memory Read Cycle
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
A0h
A0h
A0h
A15- A8 (Higher Order Address bus)
00h
21h
01h
45h
02h
F0h
DA7-DA0 (Lower order address/data Bus)
ALE
RD
WR
IO/M

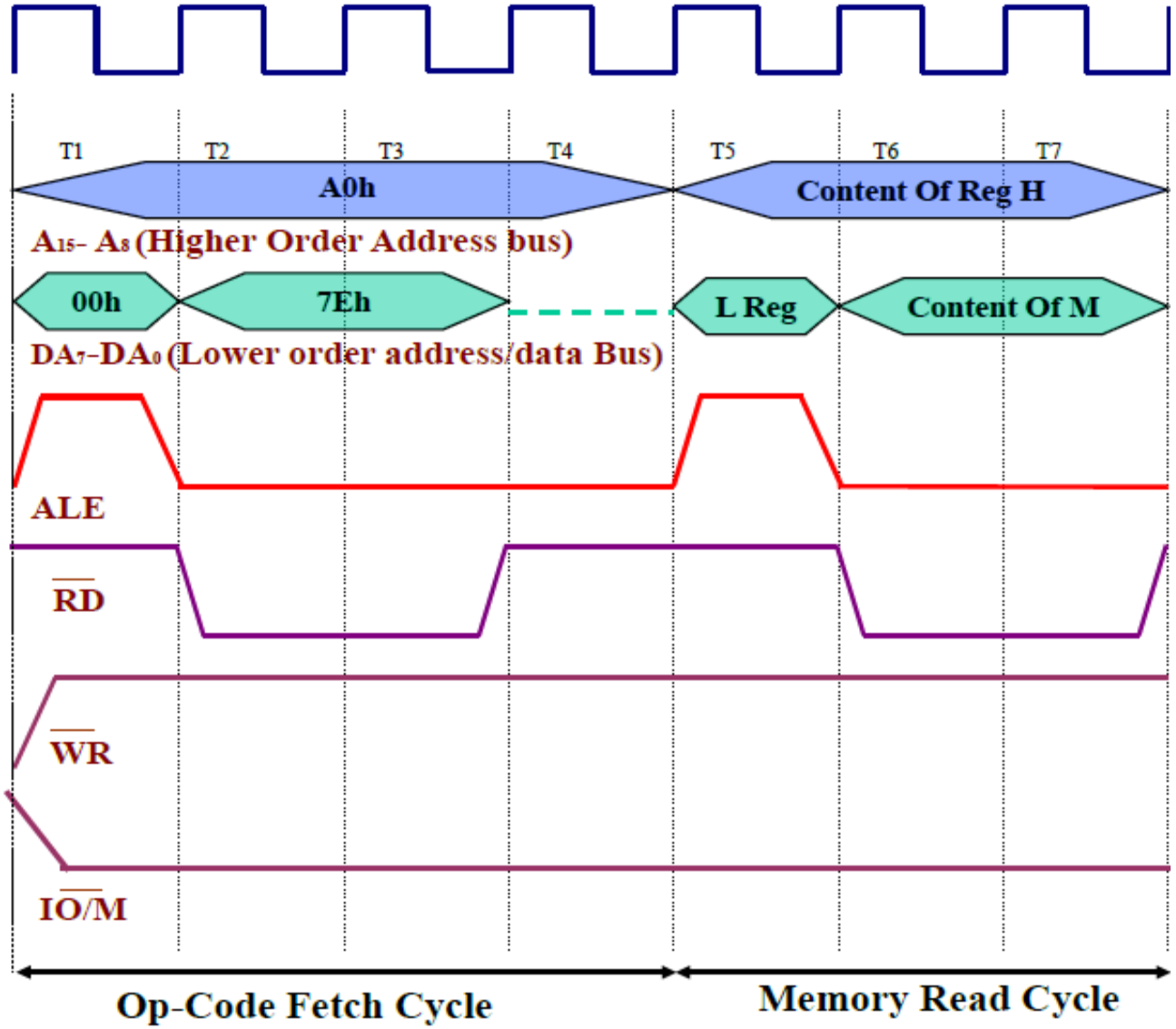


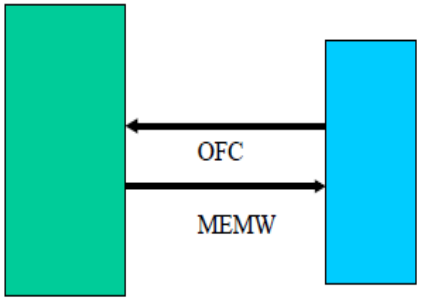
Instruction:

A000h MOV A,M

Corresponding Coding:

A000h 7E





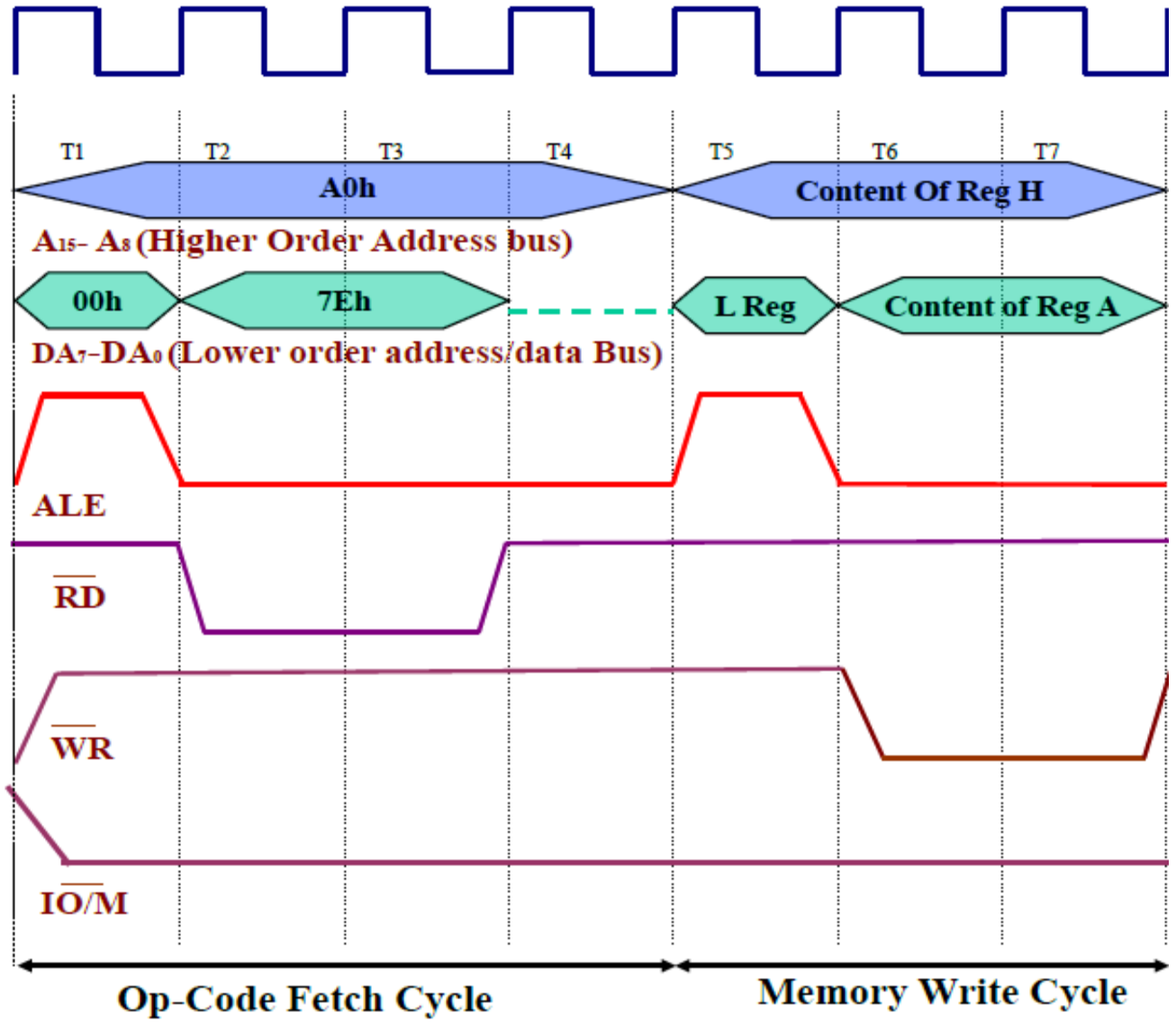
8085 Memory

Instruction:

A000h MOV M,A

Corresponding Coding:

A000h 77



STA instruction

ex: **STA 526A**

Address	Mnemonics	Opcode
41FF	STA $526A_H$	32_H
4200		$6A_H$
4201		52_H

It require 4 m/c cycles

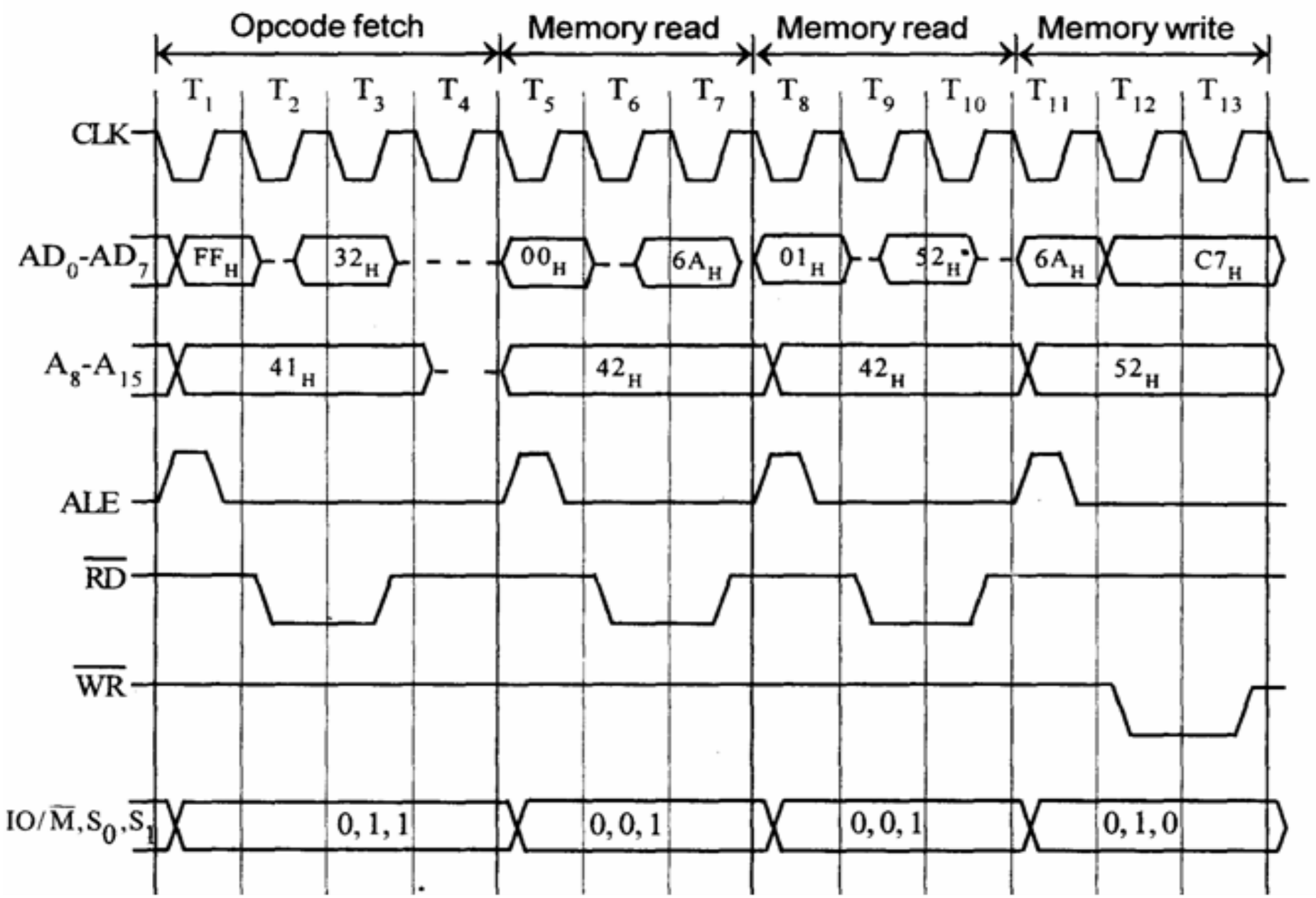
13 T states

1.opcode fetch(4T)

2.memory read(3T)

3.memory read(3T)

4.Memory write(3T)


Opcode fetch
Memory read
Memory read
Memory write
T1 T2 T3 T4 T5 T6 T7 T8 T9 T10 T11 T12 T13
CLK
AD0-AD7
FFH
32H
00H
6AH
01H
52H
6AH
C7H
A8-A15
41H
42H
42H
52H
ALE
RD
WR
IO/M, S0, S1
0, 1, 1
0, 0, 1
0, 0, 1
0, 1, 0

Timing diagram for IN C0H

- Fetching the Opcode DBH from the memory 4125H.
- Read the port address C0H from 4126H.
- Read the content of port C0H and send it to the accumulator.
- Let the content of port is 5EH.

It require 3 m/c cycles ,10 T states

opcode fetch(4T)

memory read(3T)

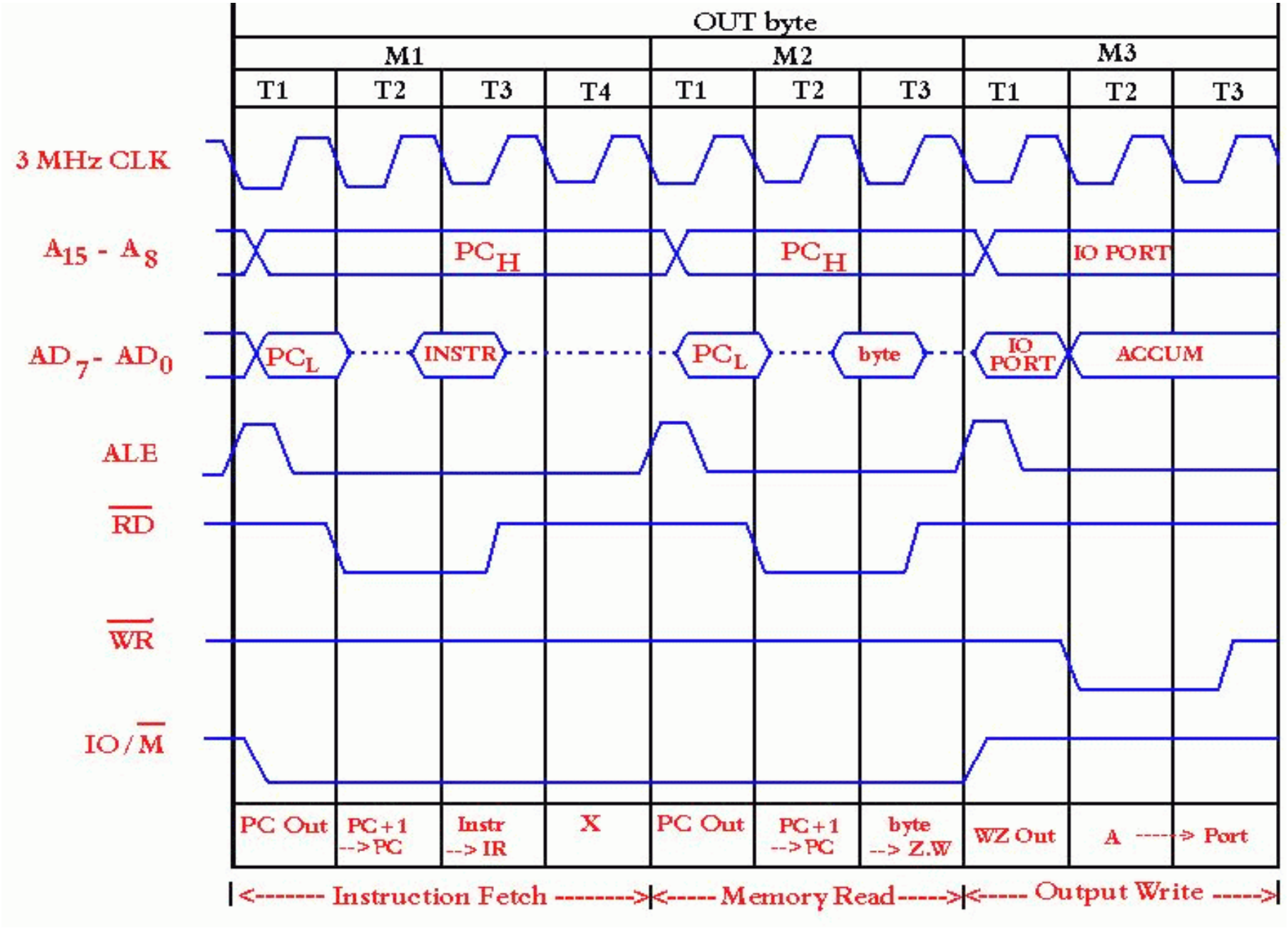
I/O read(3T)

Address	Mnemonics	Opcode
4125	IN $C0_H$	DB_H
4126		$C0_H$

OUT instruction

Machines Cycles(10T):

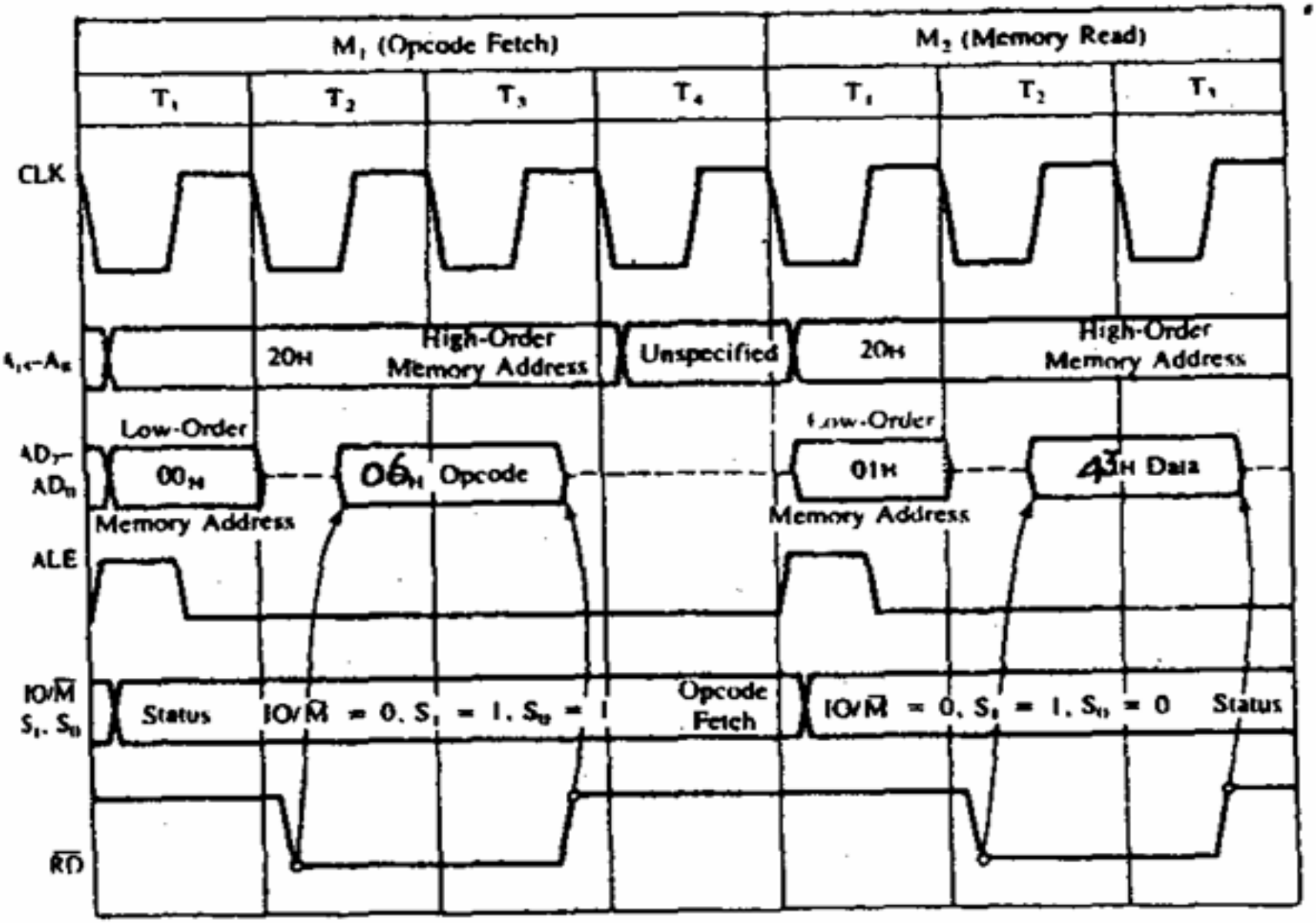
1. instruction fetch(4T)
2. memory read (3T)
3. IO write (3T)


OUT byte
M1
M2
M3
T1
T2
T3
T4
T1
T2
T3
T1
T2
T3
3 MHz CLK
A15 - A8
PCH
PCH
IO PORT
AD7 - AD0
PCL
INSTR
PCL
byte
IO PORT
ACCUM
ALE
RD
WR
IO / M
PC Out
PC+1 --> PC
Instr --> IR
X
PC Out
PC+1 --> PC
byte --> Z.W
WZ Out
A -----> Port
<------- Instruction Fetch -------->
<----- Memory Read ----->
<----- Output Write ----->

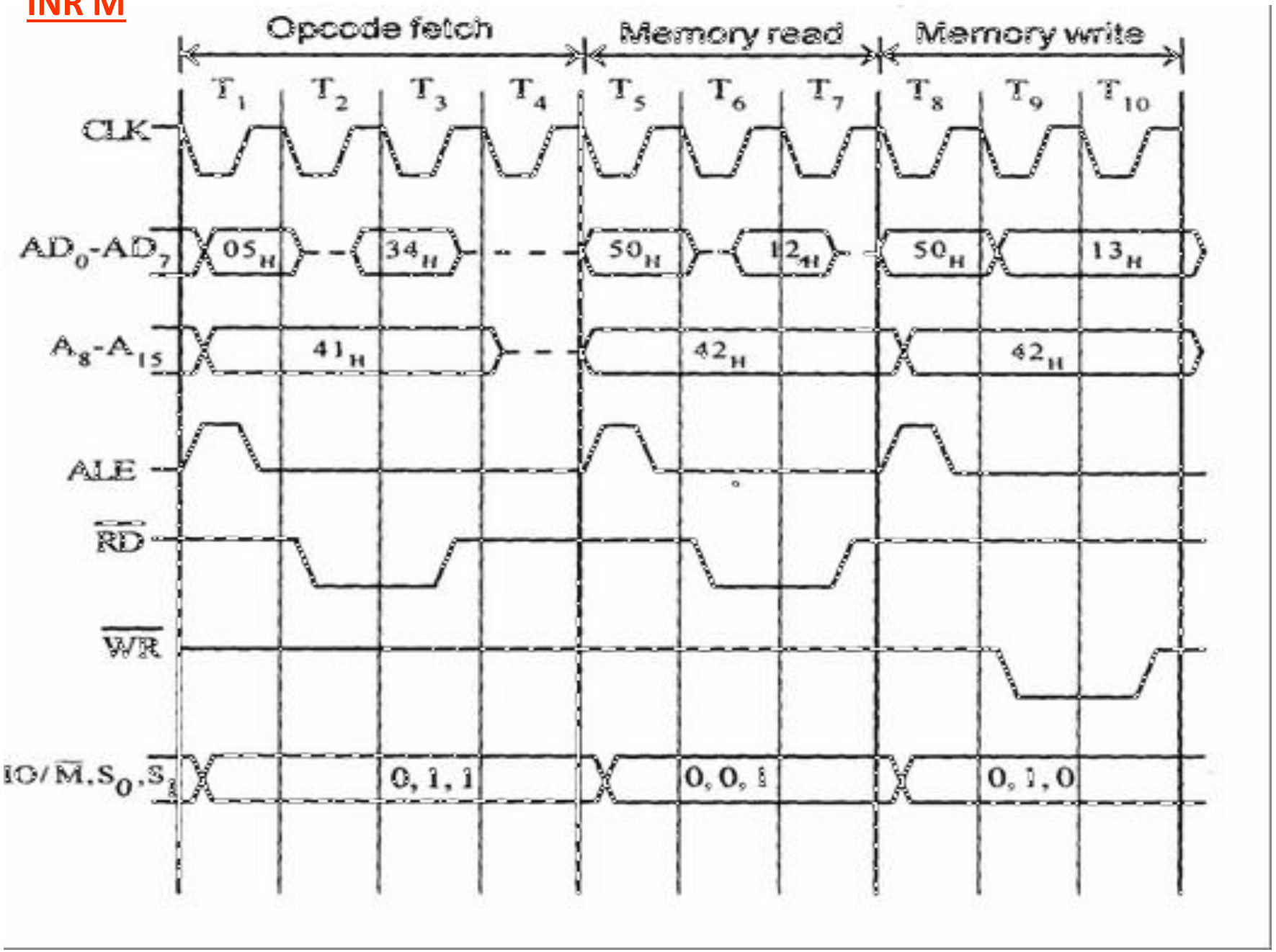
Timing diagram for MVI B, 43_h

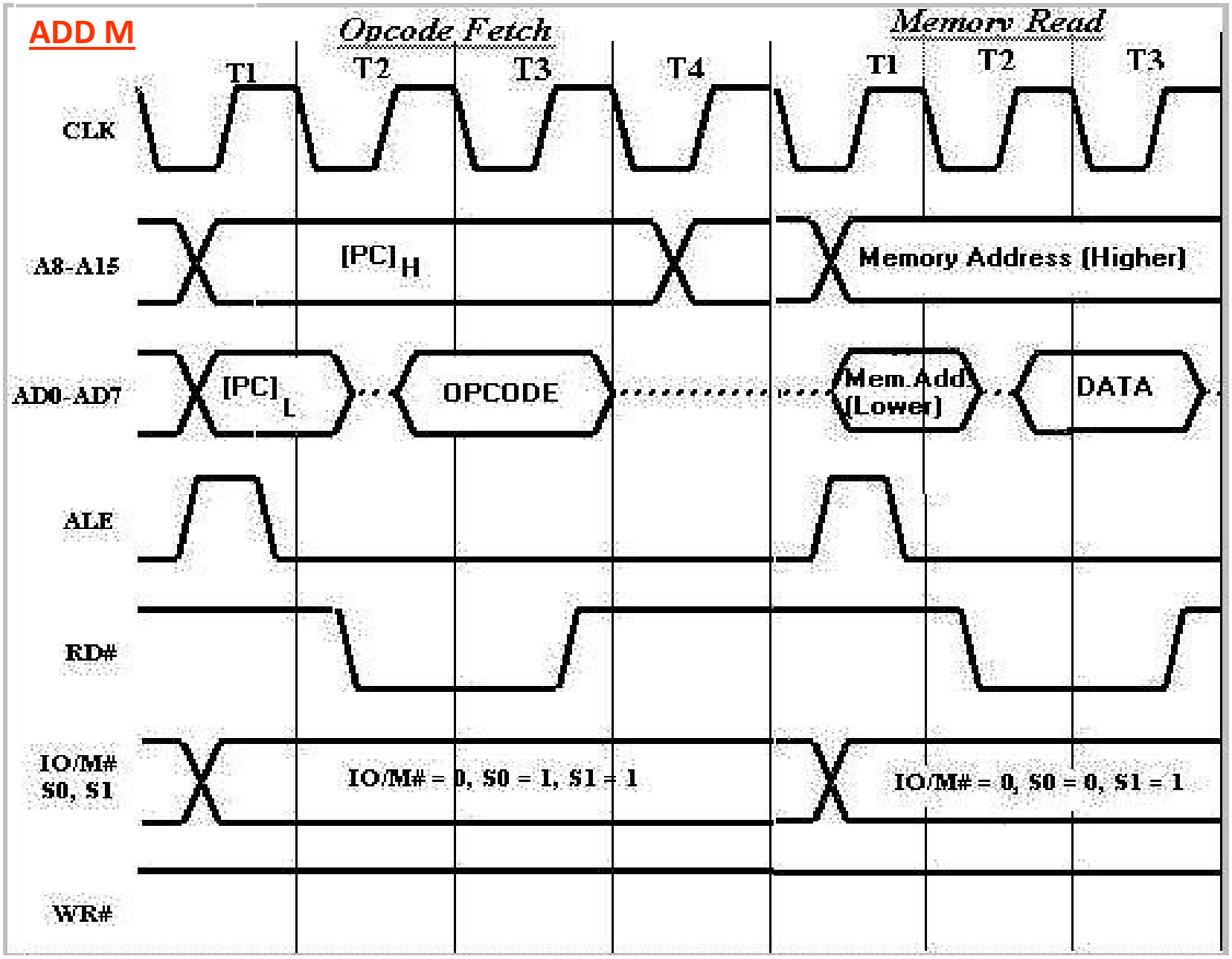
- **Fetching the Opcode 06H from the memory 2000_H. (OF machine cycle)**
- **Read (move) the data 43H from memory 2001_H. (memory read)**

Address	Mnemonics	Opcode
2000	MVI B, 43_H	06_H
2001		43_H


M1 (Opcode Fetch)
M2 (Memory Read)
T1
T2
T3
T4
T1
T2
T3
CLK
A15–A8
20H
High-Order Memory Address
Unspecified
20H
High-Order Memory Address
AD7–AD0
Low-Order
00H
Memory Address
06H Opcode
Low-Order
01H
Memory Address
43H Data
ALE
IO/M
S1, S0
Status
IO/M = 0, S1 = 1, S0 = 1
Opcode Fetch
IO/M = 0, S1 = 1, S0 = 0
Status
RD

INR M


Opcode fetch
Memory read
Memory write
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
CLK
AD0-AD7
05H
34H
50H
12H
50H
13H
A8-A15
41H
42H
42H
ALE
RD
WR
IO/M.S0.S1
0, 1, 1
0, 0, 1
0, 1, 0


ADD M
Opcode Fetch
Memory Read
T1
T2
T3
T4
T1
T2
T3
CLK
A8-A15
[PC]H
Memory Address (Higher)
AD0-AD7
[PC]L
OPCODE
Mem.Addr.
(Lower)
DATA
ALE
RD#
IO/M#
S0, S1
IO/M# = 0, S0 = 1, S1 = 1
IO/M# = 0, S0 = 0, S1 = 1
WR#

Reference Book

"**Microprocessor Architecture, Programming and Applications with 8085**",

5thEdition, Prentice Hall

by

Ramesh S. Goankar

End