8085 Microprocessor Architecture
&
Pin configuration

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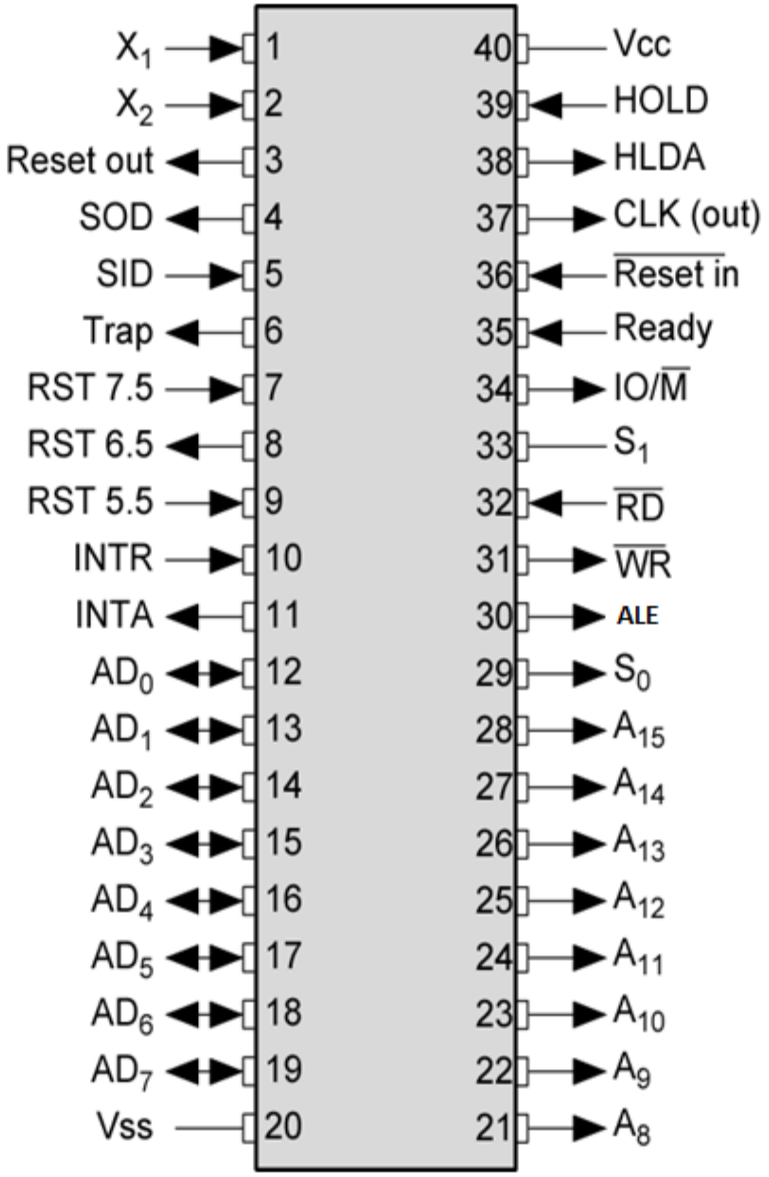
8085 Microprocessor Architecture & Pin configuration

- Pin configuration of 8085
- Limitations of 8085
- MPU Communication
- Internal Architecture of 8085
- 8085Single board Microcomputer System

Pin configuration of 8085

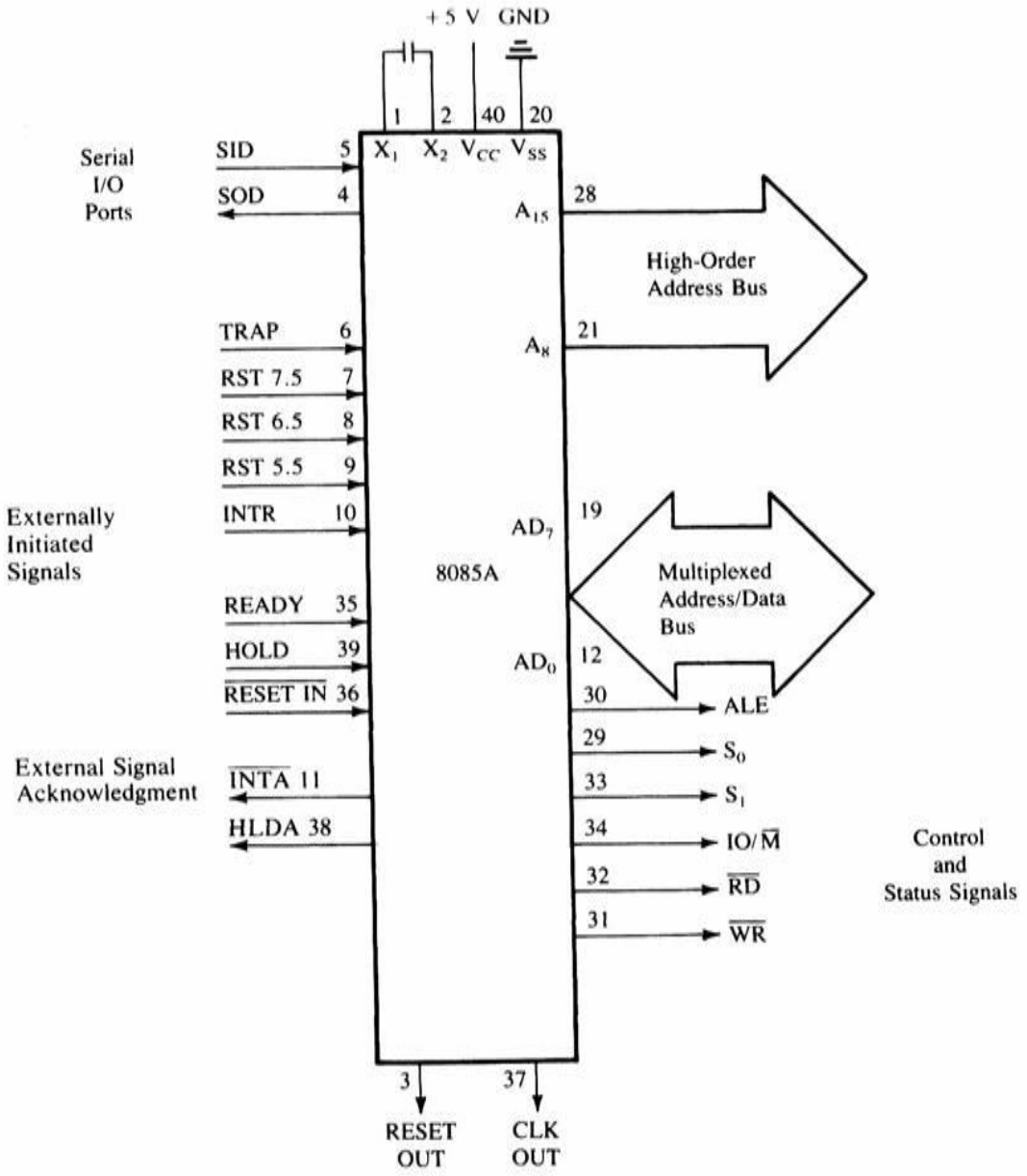


- **8-bit general purpose µp**
- **Capable of addressing 64 k of memory**
- **Has 40 pins**
- **Requires +5 v power supply**
- **Can operate with 3 MHz clock**

Pin configuration of 8085

All the signals can be classified into Six groups –

1. **Address Bus**
2. **Data Bus**
3. **Control & Status signals**
4. **Power signal & frequency signals**
5. **Externally initiated signals**
6. **Serial I/O ports**



Address & data bus

- 8085 µp consists of 16 signal pins use as address bus.
- Divide into 2 part: A15 – A8 (upper)
  AD7 – AD0 (lower).
  - **A15 – A8** : Unidirectional, known as '**high order address**'.
  - **AD7 – AD0** : bidirectional and dual purpose (address and data placed once at a time).
  - AD7 – AD0 also known as '**low order address**'.
  - To execute an instruction, at early stage AD7 – AD0 uses as address bus and alternately as data bus for the next cycle.
  - The method to change from address bus to data bus known as '**bus multiplexing**'.

Control & Status signals

This group of signal includes-

- Two control signals (**RD'** & **WR'**)
- Three status signals (**IO/M'** , **S1** & **S0**)
- One special signal (**ALE**)

- **RD'** – Read (active low). To indicate that the I/O or memory selected is to be read and data are available on the bus.

- **WR'** – Write (Active low). This is to indicate that the data available on the bus are to be written to memory or I/O ports.

- **IO/M'** – To differentiate I/O operation or memory operations.
  - '0' - indicates a memory operation.
  - '1'-indicates an I/O operation.
  - IO/M' combined with RD and WR to generate I/O and memory control signals.

Control and Status Signals.

- **S1 and S0:** Status signals, similar to IO/M, can identify various operations as shown on the following table :

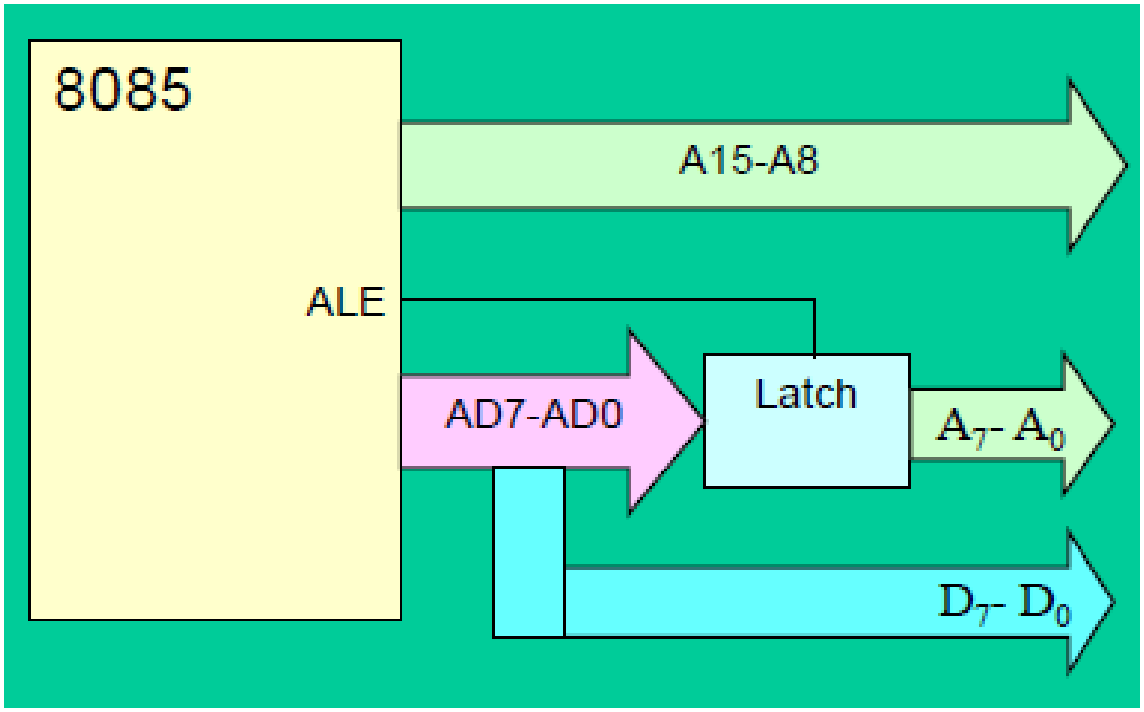
Machine Cycle	Status			Control Signals
	$IO/\overline{M}$	S_1	S_0	
Opcode Fetch	0	1	1	$\overline{RD} = 0$
Memory Read	0	1	0	$\overline{RD} = 0$
Memory Write	0	0	1	$\overline{WR} = 0$
I/O Read	1	1	0	$\overline{RD} = 0$
I/O Write	1	0	1	$\overline{WR} = 0$
Interrupt Acknowledge	1	1	1	$\overline{INTA} = 0$
Halt	Z	0	0	$\overline{RD}$, $\overline{WR}$ = Z and $\overline{INTA} = 1$
Hold	Z	X	X	
Reset	Z	X	X	

NOTE: Z = Tri-state (high impedance)
X = Unspecified

Control & Status signals

•**ALE (Address Latch Enable) signal :**

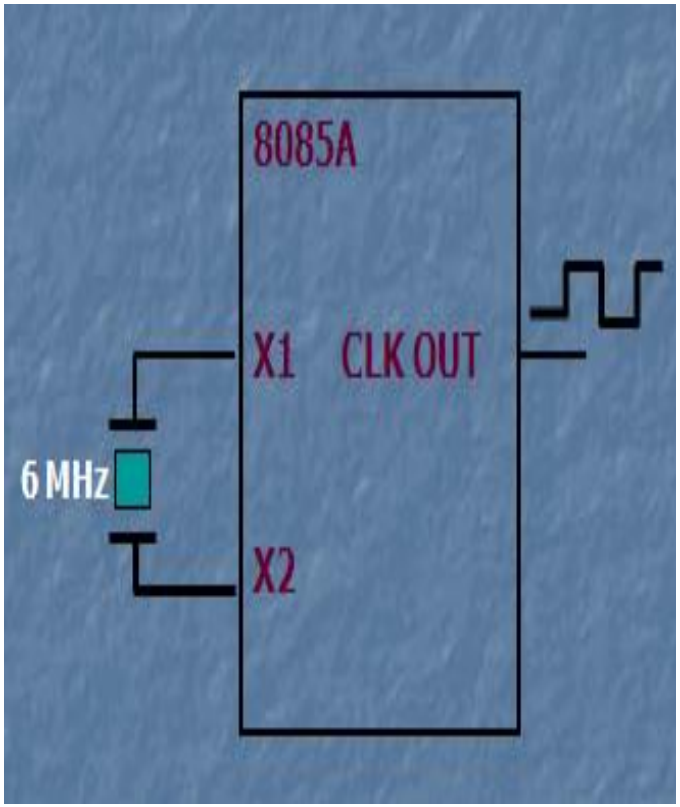
- ✓ALE used to de-multiplex address/data bus
- ✓Active high signal - generated to show the start of 8085 operation.
- ✓When transition 1-to-0: indicate that lines AD7-AD0 (AD7-AD0 = A7-A0) act as address lines.



Power signal & frequency signals

- **Vcc** : +5 V power supply
- **Vss** : Ground reference
- **X1** & **X2** : A crystal is connected at these two pins. The frequency is divided by two.

  Therefore, to operate a system at **3 MHz**, the crystal should have a frequency of **6 MHz**.
- **CLK OUT** : This signal is used as the system clock for other devices.



Externally initiated Signals including Interrupt

- ☐ INTR (Input) — Interrupt Request: This is used as a general-purpose interrupt; it is similar to the INT signal of the 8080A.
- ☐ $\overline{\text{INTA}}$ (Output) — Interrupt Acknowledge: This is used to acknowledge an interrupt.
- ☐ RST 7.5 (Inputs), RST 6.5, RST 5.5 — Restart Interrupts: These are vectored interrupts that transfer the program control to specific memory locations. They have higher priorities than the INTR interrupt. Among these three, the priority order is 7.5, 6.5, and 5.5.
- ☐ TRAP (Input) — This is a nonmaskable interrupt and has the highest priority.
- ☐ HOLD (Input) — This signal indicates that a peripheral such as a DMA (Direct Memory Access) controller is requesting the use of the address and data buses.
- ☐ HLDA (Output) — Hold Acknowledge: This signal acknowledges the HOLD request.
- ☐ READY (Input) — This signal is used to delay the microprocessor Read or Write cycles until a slow-responding peripheral is ready to send or accept data. When this signal goes low, the microprocessor waits for an integral number of clock cycles until it goes high.

Externally initiated Signals including Interrupt

- An interrupt is a hardware-initiated subroutine CALL.
- When interrupt pin is activated, an ISR will be called, interrupting the program that is currently executing.

Pin	Subroutine Location
TRAP	0024
RST 5.5	002C
RST 6.5	0034
RST 7.5	003C
INTR	*
*Note: * the address of the ISR is determined by the external hardware.*	

Externally initiated Signals including Interrupt

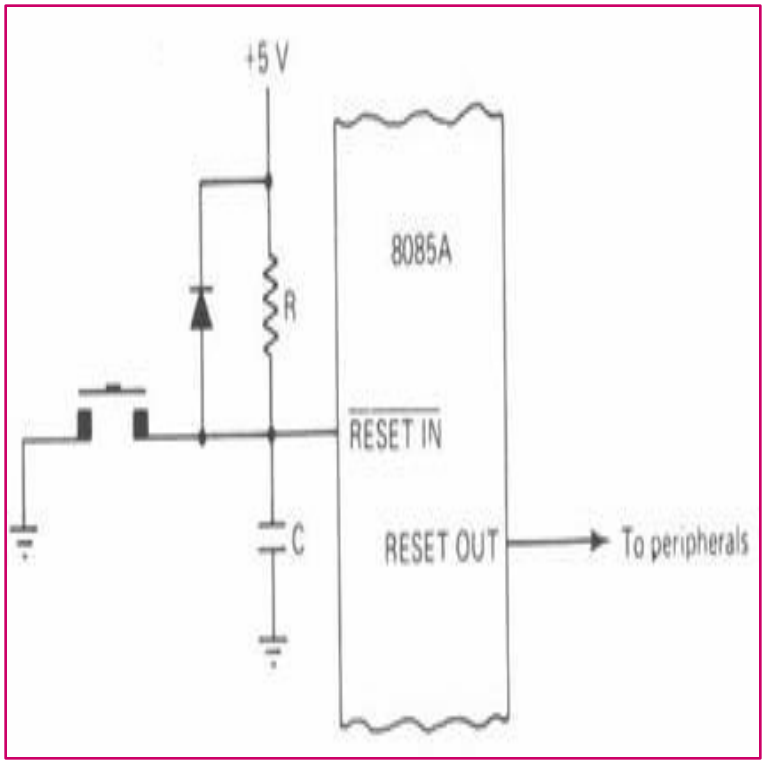
- INTR input is enabled when EI instruction is executed.
- The status of the RST 7.5, RST 6.5 and RST 5.5 pins are determined by both EI instruction and the condition of the mask bits in the interrupt mask register.

Externally initiated Signals including Interrupt

RESET IN' : When the signal on this pin goes low,

- ✓the program counter is set to zero.
- ✓the buses are tri-sated.
- ✓MPU is reset.

RESET OUT : This signal is used to reset other devices.



Serial I/O ports

The 8085 has two signals to implement the serial transmission:

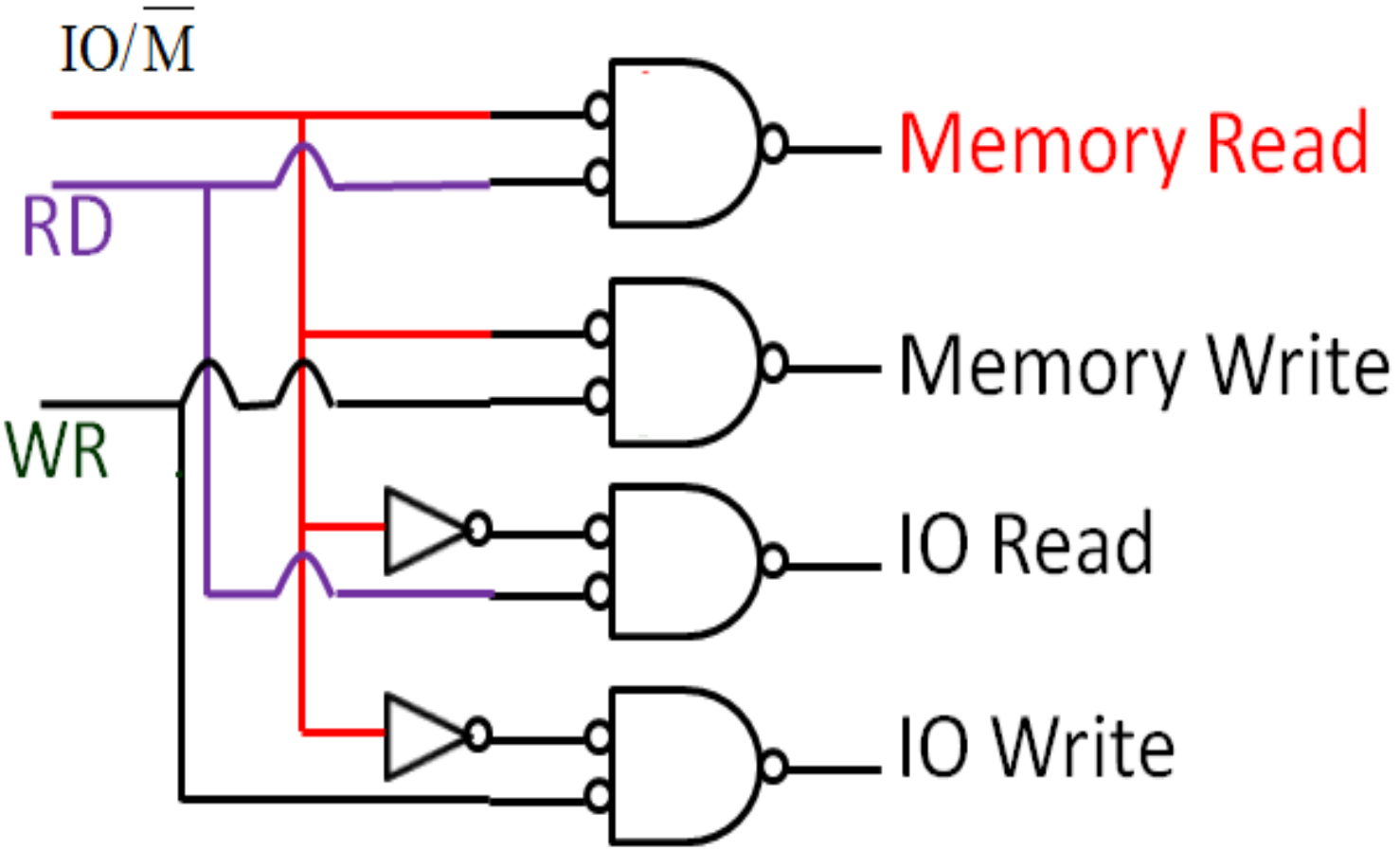
- **SID**: Serial Input Data
- **SOD**: Serial Output Data

Limitations of 8085

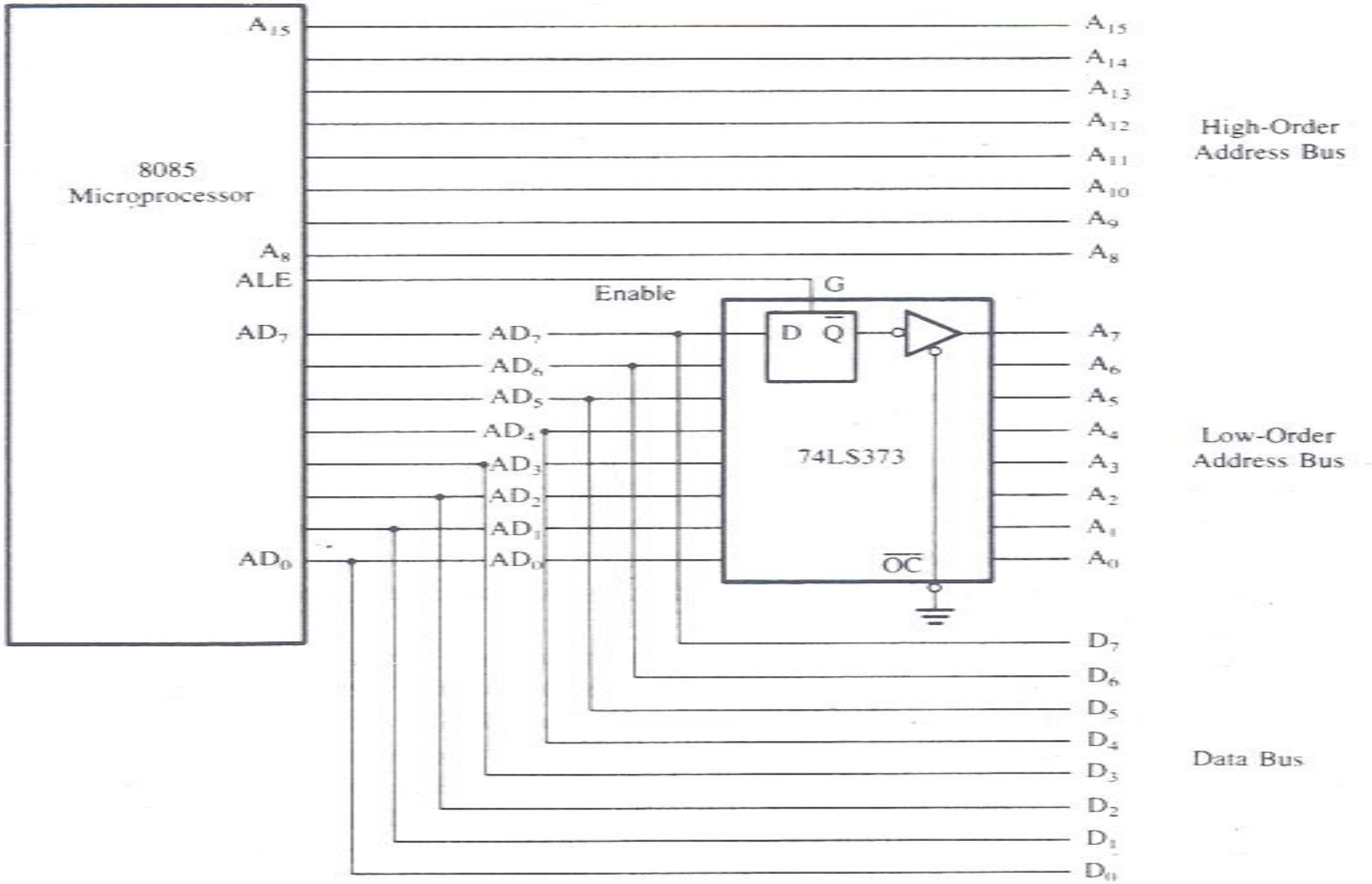
- The low order address bus is multiplexed with the data bus. The buses need to be de-multiplexed.

- Appropriate control signals need to be generated to interface memory and I/O with the 8085.

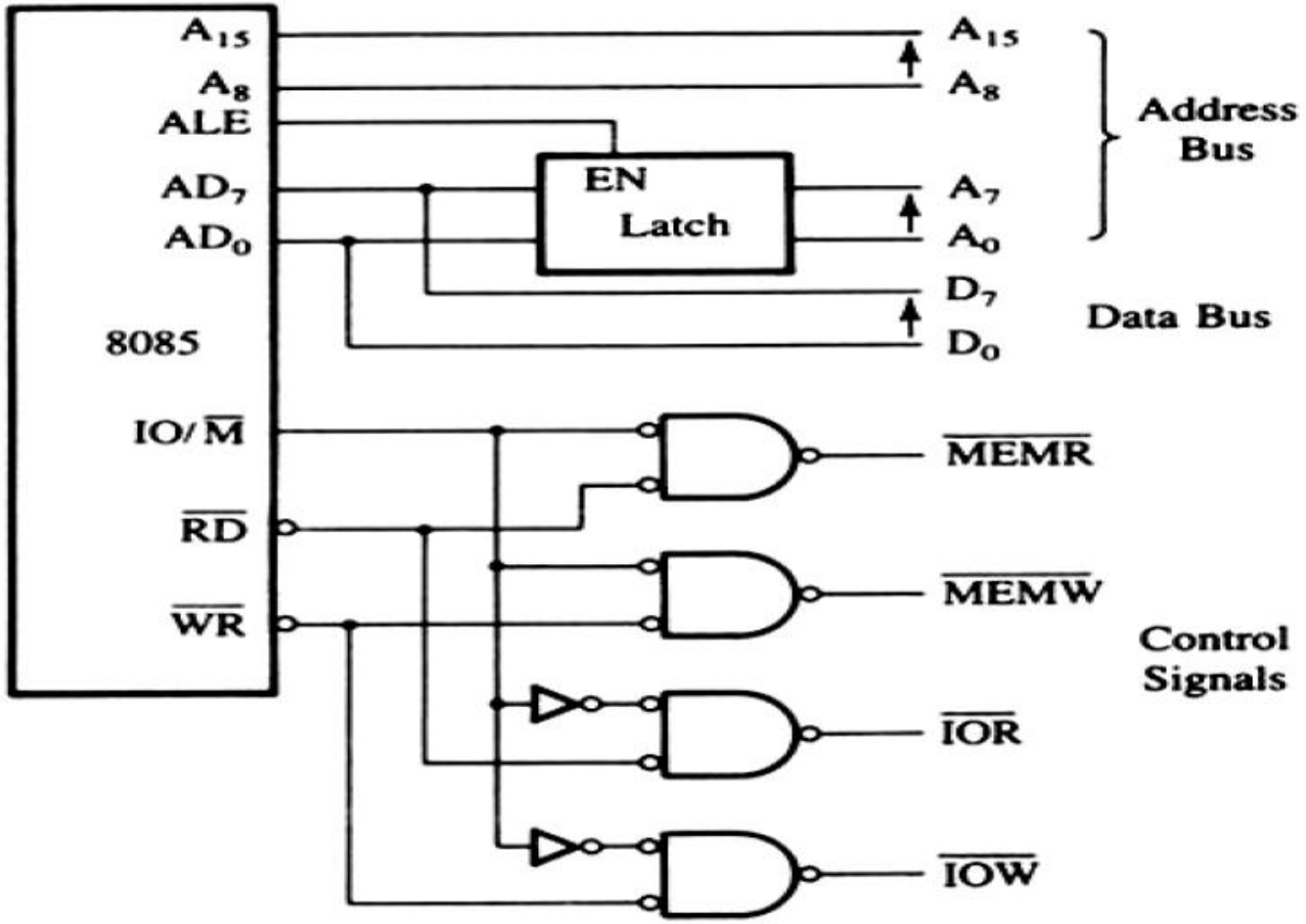
Generating Control Signals



De-multiplexing Address/Data Lines



De-multiplexed Address & Data bus with Control Signals



MPU Communication

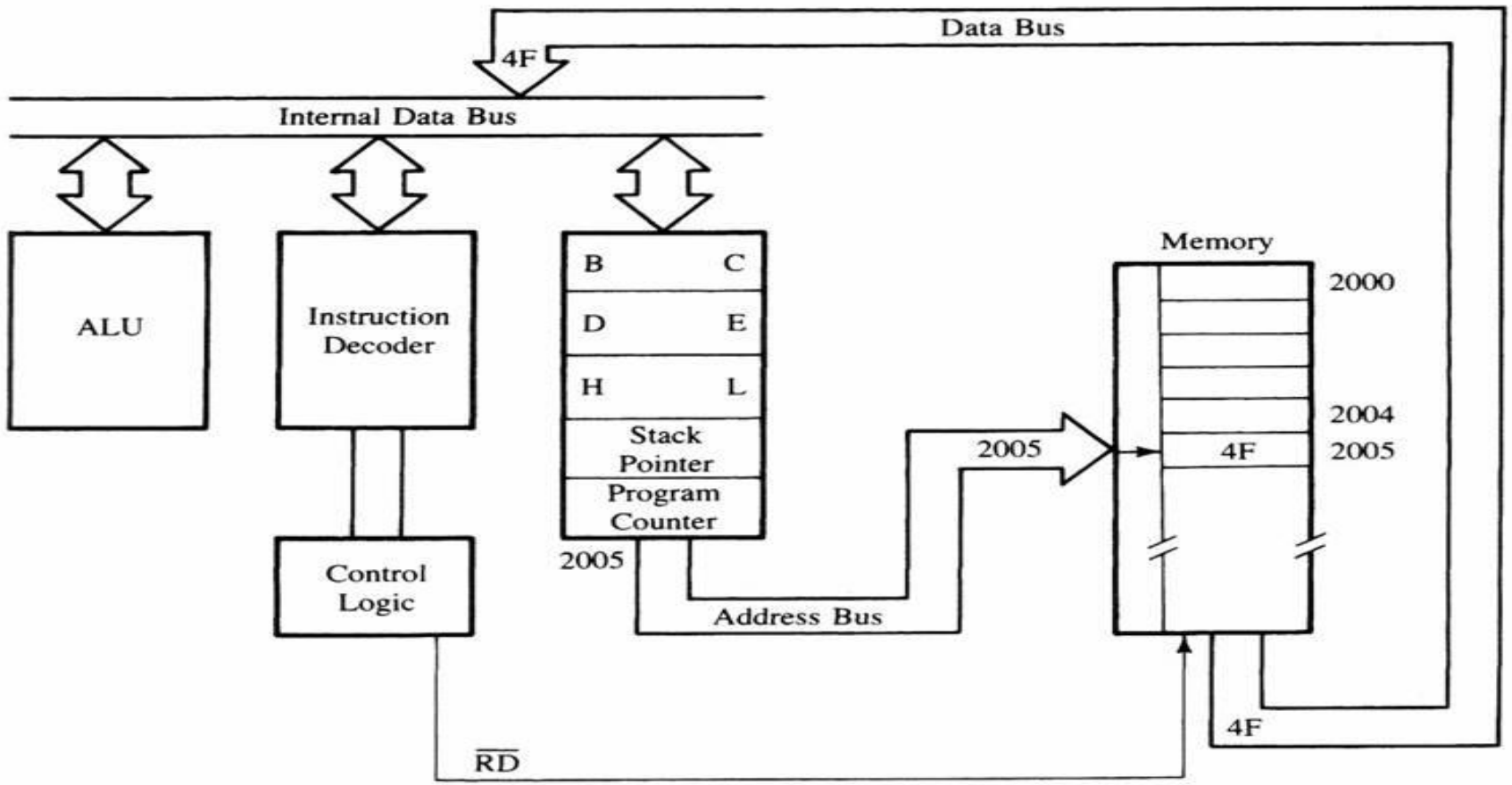


Figure : Moving data form memory to MPU using instruction **MOV C, A** (code machine 4FH = 0100 1111)

MPU Communication

1. The µp placed a 16 bit memory address from PC (program counter) to address bus.
   - The high order address, 20H, is placed at A15 – A8.
   - the low order address, 05H, is placed at AD7 - AD0 and ALE is active high.
   - Synchronously the IO/M is in active low condition to show it is a memory operation.

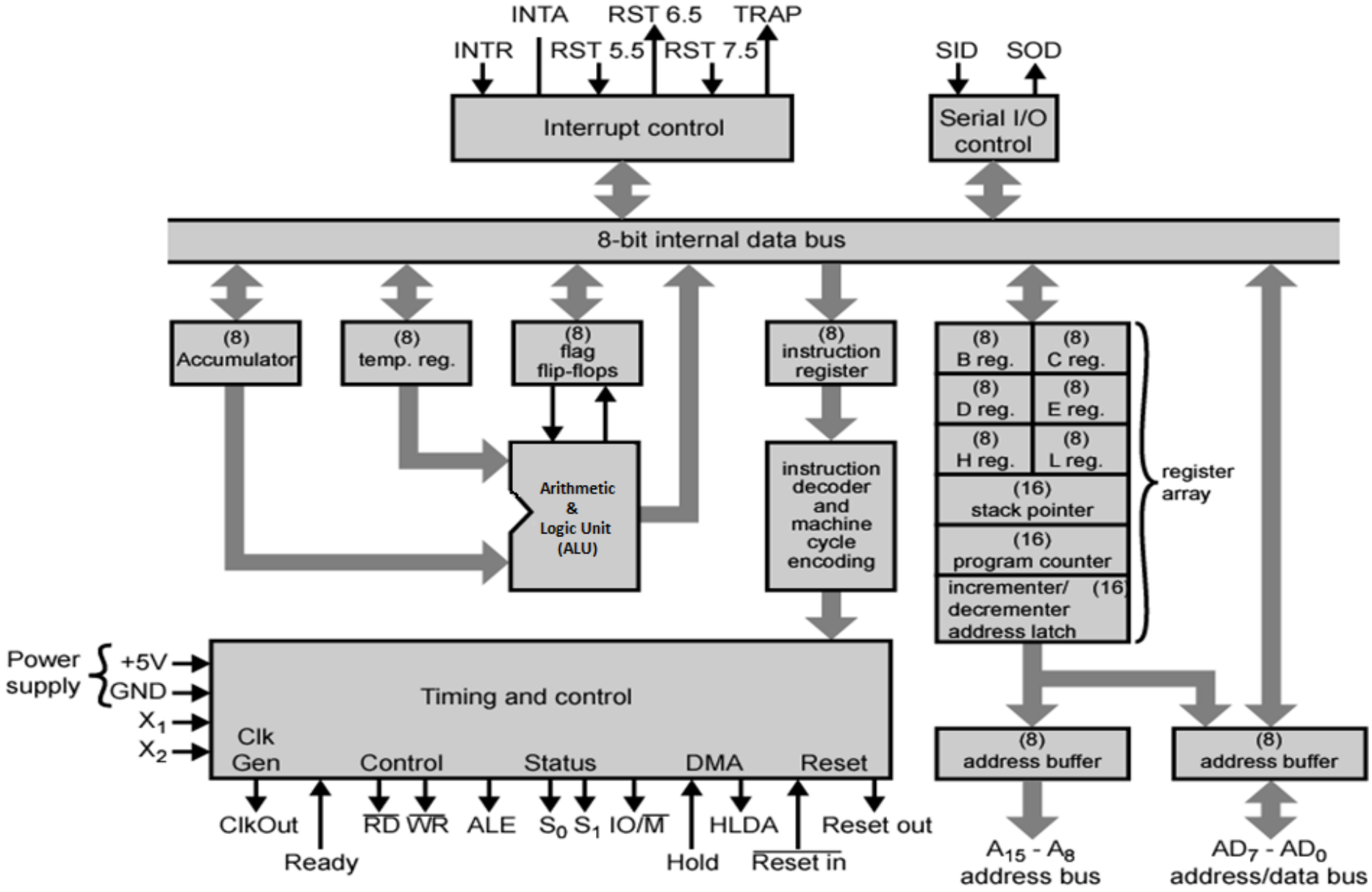
2. Then, active low control signal, RD, is activated so as to activate read operation; it is to indicate that the MPU is in fetch mode operation.

MPU Communication

3. The active low RD signal enabled the byte instruction, 4FH, to be placed on AD7 – AD0 and transferred to the MPU. While RD high, the data bus will be in high impedance mode.

4. The machine code, 4FH, will then be decoded in instruction decoder. The content of accumulator (A) will then copied into C register.

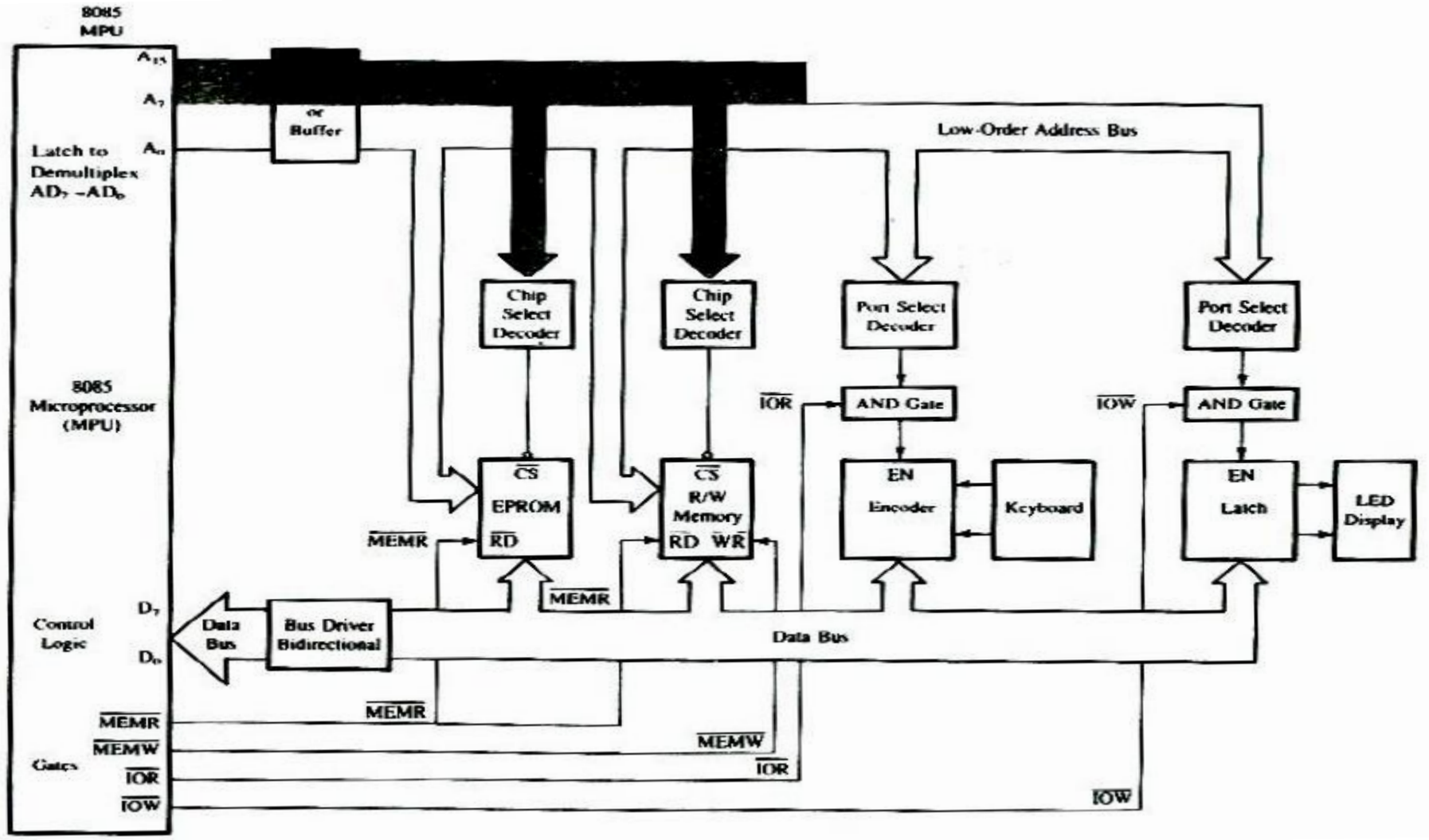
Internal Architecture of 8085



Internal Architecture of 8085

- It includes-
  - ALU
  - Timing & Control Unit
  - Instruction Register and Decoder
  - Register Array
  - Interrupt Control
  - Serial I/O Control

8085Single board Microcomputer System



Reference Book

"**Microprocessor Architecture, Programming and Applications with 8085**", 5thEdition, Prentice Hall

by

Ramesh S. Goankar

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